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IN THIS ISSUE

Minimize Standby Current in Automotive DDR Supplies

David Gilbert

When you turn on a laptop or a smart phone, you expect to wait for it to boot up, but you are less patient when you turn on your car. With a car, consumers expect immediate access to computer electronics, including navigation and infotainment systems, and automobile manufacturers strive to meet this desire with design strategies that shorten start-up time. One such strategy is to keep dynamic memory (RAM) active at all times, even during the ignition-off state.

The DDR3 memory used in automobiles operates on a 1.5V rail with peak load currents over 2A—preferably produced by a high efficiency DC/DC converter to minimize heat dissipation. In these applications, light load efficiency is just as important to preserve battery life when the automobile is not running. DDR memory can consume 1mA–10mA from the 1.5V rail in standby, but drawing 10mA from the battery is unacceptable when the car is parked for long periods.

The LT8610 keeps automotive electronics running.

This constraint rules out the use of a linear regulator, where input and output current are equal. On the other hand, a switching step-down (buck) regulator draws less input current than load current in proportion to the step-down ratio:

$$I_{IN} = \frac{1}{\eta} \bullet \frac{V_{OUT} \bullet I_{OUT}}{V_{IN}}$$

where η is the efficiency factor (0 to 1).

Figure 1 shows that the LT®8610AB synchronous step-down regulator achieves ~83% efficiency at a 1mA load. For a battery voltage of 12V and load current of 1mA at 1.5V, calculated input current is only 151µA.

(continued on page 4)

In this issue...

Linear in the News

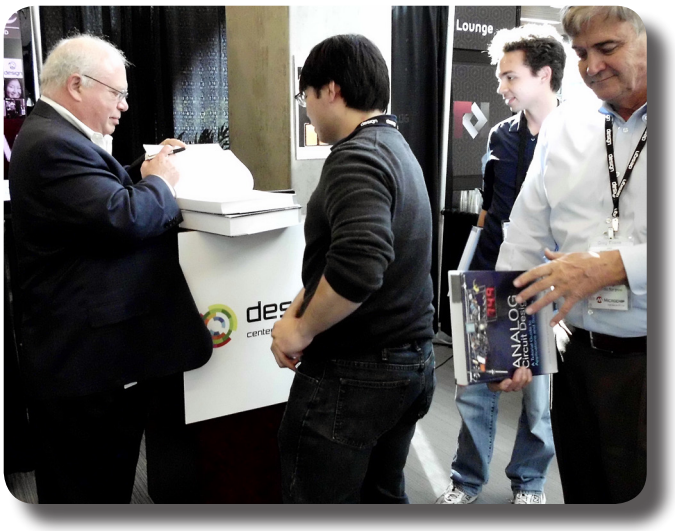
ANALOG CIRCUIT DESIGN BOOK MAKES WAVES

Published by the Newnes imprint of Elsevier Science & Technology Books in January, Linear's *Analog Circuit Design, Volume 2* is gaining readers. The book, edited by industry gurus Bob Dobkin and the late Jim Williams, is the second volume of the series, covering a broad range of analog circuit design techniques. *Analog Circuit Design, Volume 2, Immersion in the Black Art of Analog Design* has received positive reviews in various electronics publications. *EDN* is currently running excerpts of the book's chapters on their website.

EDN Analog and Power editor Steve Taranovich commented, "This book is a great companion volume to Volume I with informative application notes and a full complement of reference designs. The chapters are not just every day application notes and reference designs, but give insights into problem-solving, design decision-making, the thought process that goes along with a robust, successful design. That's why I love this book. The authors, Bob Dobkin and the late Jim Williams (along with the research and writings of Carl Nelson and Bob Widlar), have a rich history and depth of experience that they share with the readers. This book is a keeper that needs to be on every designer's bookshelf, right next to Volume I."

A recent article in UK's *Electronics Weekly* commented, "It is a book that delves into the deepest subtleties of linear analog electronics and, unless you have no imagination, and just want to copy a reference design, or you are already a grade-A analog guru, you will learn something from every page."

In April, at the Design West Show, held in San Jose, California, Bob Dobkin discussed the art of analog design, took questions from engineers and signed copies of both volumes of the *Analog Circuit Design* book series. On display, along with



Bob Dobkin signs *Analog Circuit Design, Volume 2* at Design West

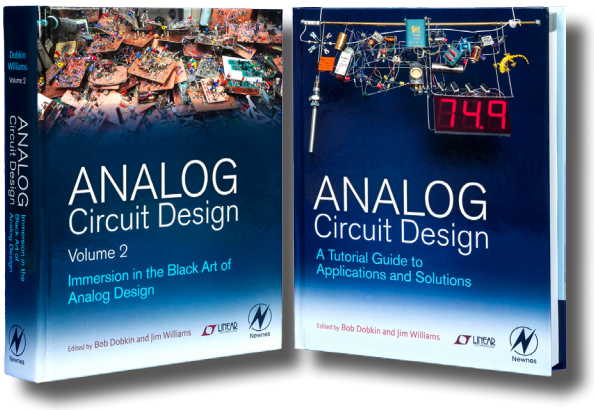
the book, were photos of Jim Williams' innovative electronic sculpture art, which Jim painstakingly assembled from found electronics that he personally scoured from his frequent trips to electronics flea markets. In addition to being a work of art, each of Jim's sculptures is a working electronic instrument, providing accurate readings of temperature, barometric pressure and other natural phenomena.

At the book signing, Bob Dobkin discussed the challenges and satisfactions of analog circuit design. Following is an excerpt from Bob Dobkin's Foreword to *Analog Circuit Design, Volume 2*:

"Analog design is challenging. There are many ways to get from input to output, and the circuitry in the middle can lead to divergent results. Analog design is like learning a language. When you first learn a language, you begin with a vocabulary book and then analyze writings in that language by looking up words one by one as you encounter them. Likewise, in analog design you learn the basics of the circuit, as well as the function of different devices. You can write node equations and determine what the circuit is doing by studying each of the individual circuits.

"With analog circuit design, you end up using the basic circuit configurations you have learned—differential amplifiers, transistors, FETs, resistors, and previously studied circuits—to achieve the final circuit. As with a new language, it takes many years to learn to write poetry, and the same is true of analog circuit design.

"Today's system manuals rarely have any circuit design. They contain block diagrams and hookup schematics with thousands of leads to different blocks. So where do people go for analog circuit design? If you're just starting, or if you encounter a problem that's outside your experience, appropriate references are difficult to find. Hopefully, these books provide some answers, as well as circuit design and test and lab techniques for design and duplication of the circuits.



Linear's *Analog Circuit Design* book series, published by Elsevier. Volume 1 was Elsevier's best selling engineering title last year and Volume 2, published in January, is off to a strong start.

"Today, analog design is in greater demand than ever before. Analog design is now a combination of transistors and ICs that provide high functionality in analog signal processing. This volume focuses on fundamental aspects of circuit design, layout, and testing. It is our hope that the talented writers of these application notes shed some light on the 'black art' of analog design."

For more information on the book, including author videos and ordering information, visit www.linear.com/designtools/acd_book.php

LINEAR PRODUCTS RECEIVE AWARDS

Several Linear products have recently been honored with significant industry awards:

EE Times & EDN ACE Award for Best Power Device, LTC6804 Battery Stack Monitor—The LTC®6804 is a high voltage battery monitor for hybrid electric and electric vehicles, and other high voltage, stacked-battery systems. An LTC6804 can measure up to 12 series-connected battery cells at voltages up to 4.2V with 16-bit resolution and better than 0.04% accuracy.

EE Times China ACE Award for Best Power Management Product, LT8610/LT8611—The LT8610 is a 2.5A, 42V input capable synchronous step-down switching regulator. Synchronous rectification delivers efficiency as high as 96% while Burst Mode® operation technology keeps quiescent current under 2.5µA in no load standby conditions. The device's ultralow quiescent current makes it well suited for applications such as automotive or industrial systems, which demand always-on operation and optimum battery life.

EE Times China ACE Award for Best Data Conversion Product, LTC2389-18—The LTC2389-18 is the fastest 18-bit no latency SAR ADC on the market with unrivaled 99.8dB SNR at 2.5Msps. The device's high precision makes it ideal for applications in medical imaging, high speed data acquisition, scientific instrumentation, industrial process control, automatic test equipment, radar, sonar and semiconductor production equipment.

CONFERENCES & EVENTS

Techno Frontier 2013, Power System Show, Tokyo Big Sight, Tokyo, Japan, July 17-19, Booth 1F301—Linear will showcase high performance analog solutions, with products displayed in power system management, battery management systems and wireless sensor networks. More at www.jma.or.jp/tf/en/index.html

The Battery Show 2013, Suburban Collection Showcase, Novi, Michigan, September 17-19, Booth E1011—Presenting Linear's battery management system products. Sam Nork will present "Active balancing solutions for series-connected battery packs" at 12:05 pm, Thursday, September 19. More at www.thebatteryshow.com ■

The LT8610A and LT8610AB have a low component count, low minimum input voltage, low quiescent current and high efficiency across a wide load range. These features make them the preferred solution for providing standby power to DDR memory in automotive applications.

(LT8610A/AB continued from page 1)

DIRECT DC/DC CONVERSION FROM CAR BATTERY TO 1.5V DDR MEMORY

LT8610A and LT8610AB are monolithic, synchronous step-down regulators designed specifically for automotive systems. They deliver 3.5A while consuming only 2.5µA quiescent current. Building a circuit around them is easy. No additional semiconductors are required, they work with inexpensive ceramic capacitors, and the MSOP package has leads that are easy to solder and inspect. With a typical minimum on-time of 30ns (45ns guaranteed maximum), one can design compact, high switching-frequency buck regulators with large step-down ratios. Figure 2 shows an application that delivers 3.5A at 1.5V. The operating frequency is 475kHz to optimize efficiency and remain below the AM radio band.

Both parts feature excellent fault tolerance to automotive environments. A maximum input of 42V handles load dumps. A robust switch design and high speed current comparator protect the device during output shorts. The minimum input is worst-case 3.4V, the maximum duty cycle is above 99% and the dropout voltage is typically 200mV at 1A, all of which keep the output in regulation through cold-crank. The typical minimum input voltage is plotted in Figure 3.

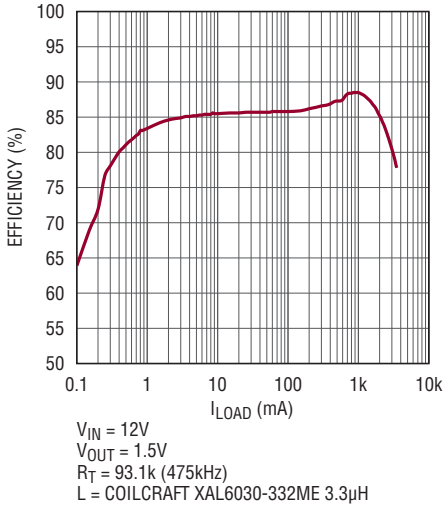


Figure 1. LT8610AB efficiency versus load

SAVE THE BATTERY WITH LOW RIPPLE Burst Mode OPERATION AND MINIMAL QUIESCENT CURRENT

The LT8610A and LT8610AB are designed to minimize output voltage ripple over the entire load range. At light loads, they maintain efficiency by reducing their operating frequency and entering Burst Mode® operation. Fast transient response is maintained even at very low loads. This feature combined with the very low quiescent current of 2.5µA means that, even at a few µA of load, the LT8610A and LT8610AB are more efficient than a linear regulator with zero quiescent current. For systems where low frequency operation must be avoided, Burst Mode operation can be turned off by applying either a logic high signal or clock signal to the SYNC pin.

The difference between the LT8610A and LT8610AB is that the LT8610AB features higher efficiency at light loads. This is achieved by using an increased Burst Mode current limit, allowing more energy to be delivered during each switch cycle and lowering the switching frequency for a given load. Because a fixed amount of energy is required to

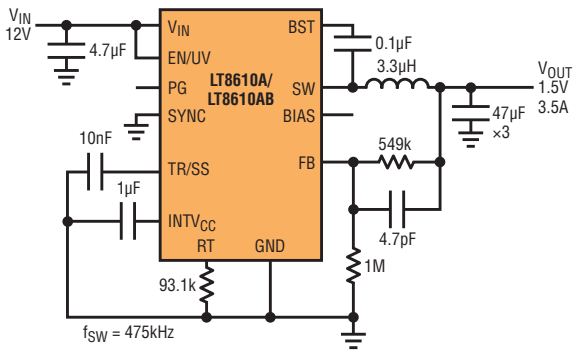


Figure 2. This LT8610A or LT8610AB step-down converter circuit accepts automotive battery and generates 1.5V at 3.5A. Low quiescent current and synchronous rectification result in high efficiency across the entire load range.

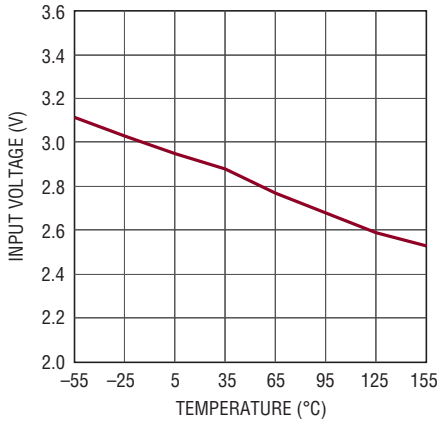


Figure 3. Keeping the memory alive in cold-crank or start-stop events. The LT8610A and LT8610AB operate down to a typical minimum input voltage of 2.9V at 25°C, with 3.4V maximum guaranteed over temperature.

The LT8610A and LT8610AB are designed to minimize output voltage ripple over the entire load range. At light loads, they maintain efficiency by reducing their operating frequency and entering Burst Mode operation. Fast transient response is maintained even at very low loads.

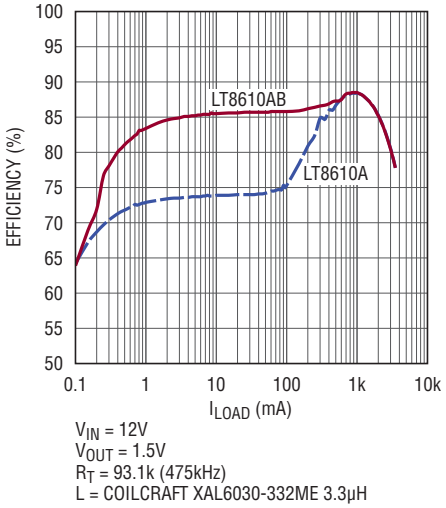


Figure 4. An increased Burst Mode current limit on the LT8610AB results in substantial efficiency gains at light load compared to the LT8610A.

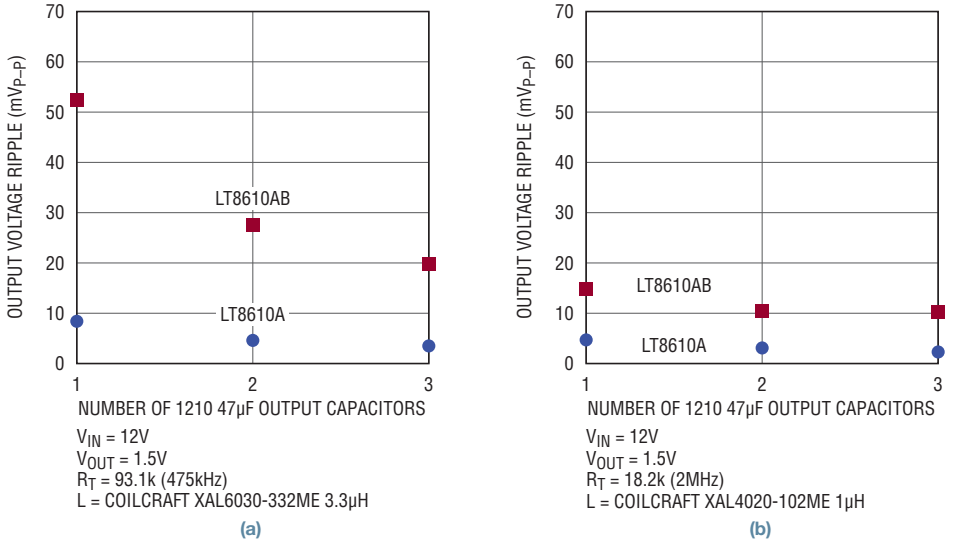


Figure 5. Output voltage ripple versus number of 1210 size 47µF output capacitors for two inductor values, at 10mA load. (a) Ripple for the 475kHz application in Figure 2. (b) Ripple for the 2MHz application in Figure 6.

switch the MOSFET on and off, a lower switching frequency reduces gate-charge losses and increases efficiency.

Figure 4 shows the efficiency difference between the LT8610A and LT8610AB. For loads between 1mA and 100mA, the LT8610AB improves efficiency by more than 10% compared to the LT8610A. The trade-off to the increased Burst Mode current limit is that more energy is delivered in each switch cycle, so more output capacitance is required to keep output voltage ripple low. Figure 5 compares the output ripple for the LT8610A and LT8610AB as a function of the output capacitance for two inductor values, at 10mA load.

In addition to the current limit, the inductor choice affects the efficiency and switching frequency in Burst Mode operation. This is because for a fixed current limit, a larger inductor value can store more energy than a smaller one. If high efficiency at light loads is paramount, then the inductor value can be increased beyond the starting value recommended in the data sheet.

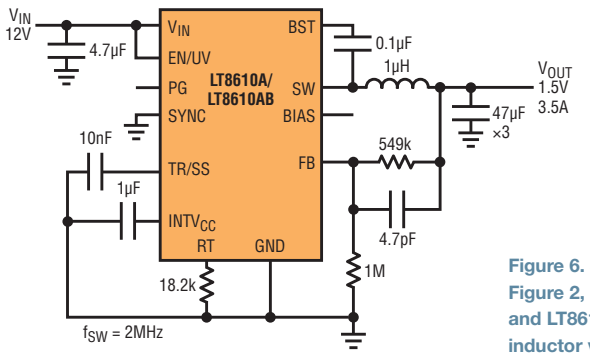


Figure 6. Similar 12V to 1.5V application as in Figure 2, but the operating frequency of the LT8610A and LT8610AB is increased to 2MHz for reduced inductor value and size.

GO FASTER FOR A SMALLER SOLUTION

For most automotive systems, 9V to 16V is the typical input voltage, so application circuits are usually optimized for this range. The 475kHz application in Figure 2 operates at the designed frequency over the entire input range of 3.5V to 42V. However, if we restrict the normal operating voltage to 16V (42V transient), the operating frequency can be increased and the value and size of the inductor reduced. With a worst-case minimum on-time of 45ns, the LT8610A and LT8610AB can be programmed to 2MHz as shown in Figure 6.

An important feature is that this internal regulator can draw current from either the V_{IN} pin or the BIAS pin. If a voltage of 3.1V or higher is tied to the BIAS pin, gate drive current is drawn from BIAS. If the BIAS voltage is lower than V_{IN}, the internal linear regulator will run more efficiently using the lower voltage supply, thus increasing overall efficiency.

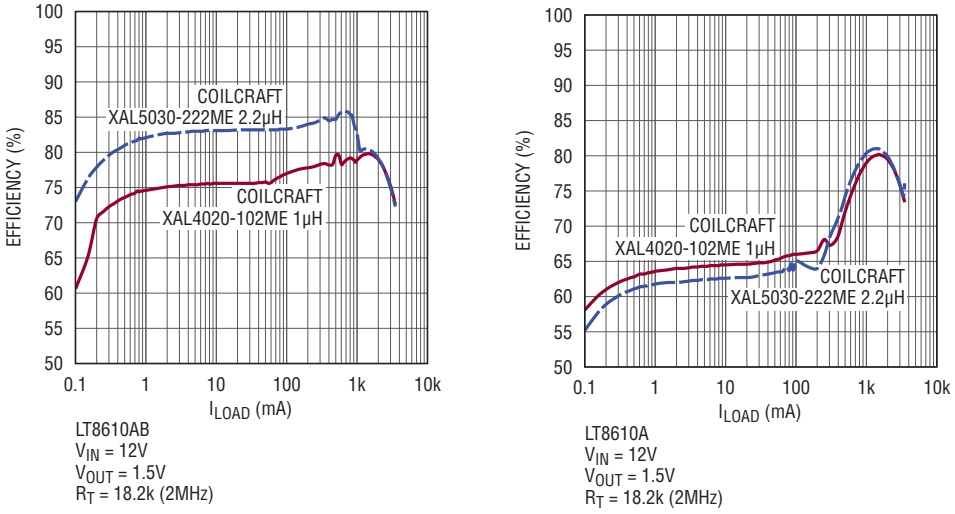


Figure 7. LT8610A and LT8610AB efficiency versus load at 2MHz with two inductor values

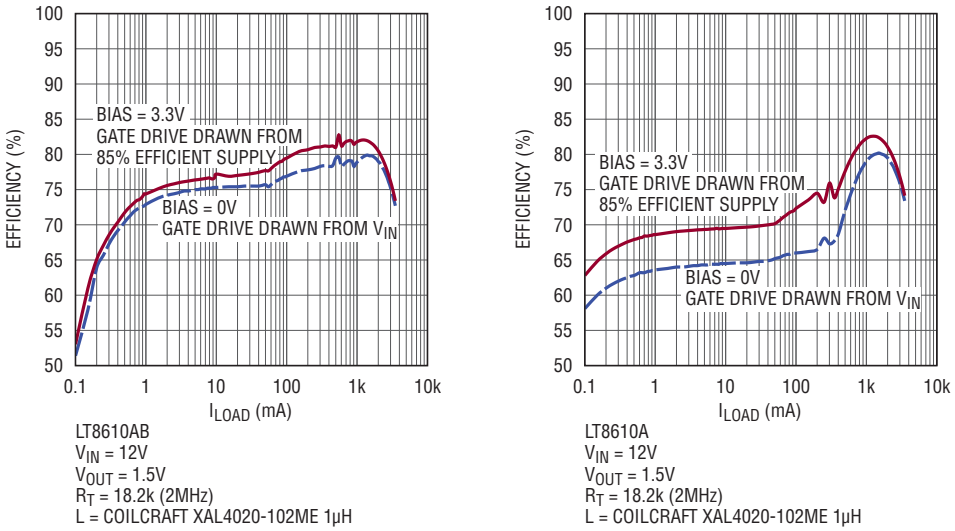


Figure 8. Efficiency can be increased if the BIAS pin is tied to an external 3.3V supply. (External supply efficiency of 85% is assumed and factored into overall efficiency shown here.)

Note that when the input voltage goes above 16V, the output remains in regulation although the switching frequency decreases to maintain safe operation. The 2MHz solution is identical to the circuit in Figure 2, except for the RT resistor changed to 18.2kΩ and the inductor value and size reduced in order to save space. Figure 7 shows efficiency versus load for two inductor choices.

BIAS PIN OPTIMIZES EFFICIENCY

The LT8610A and LT8610AB use two internal NMOSFETs specifically optimized for automotive applications. In particular, the gate drive circuitry requires less than 3V to fully enhance the FETs. To generate the gate drive supply, the LT8610A/AB includes an internal linear voltage regulator, the output of which is the $INTV_{CC}$ pin (do not load $INTV_{CC}$ with external circuitry).

An important feature is that this internal regulator can draw current from either the V_{IN} pin or the BIAS pin. If the BIAS pin is left open, then gate drive current is drawn from V_{IN}. However, if a voltage of 3.1V or higher is tied to the BIAS pin, gate drive current is drawn from BIAS. If the BIAS voltage is lower than V_{IN}, the internal linear regulator will run more efficiently using the lower voltage supply, thus increasing overall efficiency.

The efficiency data in Figures 1, 4 and 7 was recorded with the BIAS pin open. After all, if the 1.5V output is the only rail alive, then there is likely no good place to tie the BIAS pin. However, if there is a 3.3V or 5V supply, tie it to the BIAS pin, even if the supply is not available in standby or ignition-off conditions. Figure 8 shows the efficiency with and without a 3.3V supply connected to BIAS. In calculating the total efficiency, we have included the power drawn from the 3.3V rail and assumed that it was generated with 85% efficiency.

Note that the benefit to externally powering BIAS is greater at higher operating frequencies because the gate drive current is higher. The LT8610A also benefits

An important consideration for automotive applications is the behavior of the power supply during cold crank and idle-stop transients, when the voltage from the 12V battery may drop below 4V. The LT8610AB operates up to 99% duty cycle, providing output regulation at the lowest possible input voltage.

more from external bias compared to the LT8610AB—the AB's increased Burst Mode current limit results in a lower operating frequency for a given load.

NOT JUST FOR MEMORY

The LT8610AB is an excellent regulator for other automotive supplies, including 3.3V and 5V supplies, with efficiency above 90%, as shown in Figure 9.

An important consideration for automotive applications is the behavior of the power supply during cold crank and idle-stop transients, when the voltage from the 12V battery may drop below 4V. The LT8610AB operates up to 99% duty cycle, providing output regulation at the lowest possible input voltage. Figure 10(a) shows the dropout voltage. This is the difference between V_{IN} and V_{OUT} as the input voltage decreases towards the intended output regulation voltage. The LT8610AB also has excellent start-up and dropout behavior, resulting in predictable and reliable output voltage as a function of input voltage. Figure 10(b) shows the output voltage as the input supply is ramped from zero to 10V and back to zero.

CONCLUSION

The LT8610A and LT8610AB have a low component count, low minimum input voltage, low quiescent current and high efficiency across a wide load range. These features make them the preferred solutions for providing standby power to DDR memory in automotive applications. Table 1 summarizes the performance of the LT8610 family.

Visit www.linear.com/LT8610 for data sheets, demo boards and other applications information. ■

Table 1. Comparison of features for the LT8610 family of monolithic, synchronous buck converters

PARAMETER	CONDITIONS	LT8610	LT8610A	LT8610AB
Max Load Current (A)		2.5	3.5	3.5
Minimum On-Time (ns) (Typ)		50	30	30
Efficiency (%)	V_{IN} = 12V, V_{OUT} = 1.5V, I_{LOAD} = 10mA, f_{SW}=475kHz, L = 3.3µH	73.9	73.9	85.5
Output Voltage Ripple (mV_{P-P})	I_{LOAD} = 10mA, C_{OUT} = 47µF, L = 3.3µH	8.4	8.4	52.5

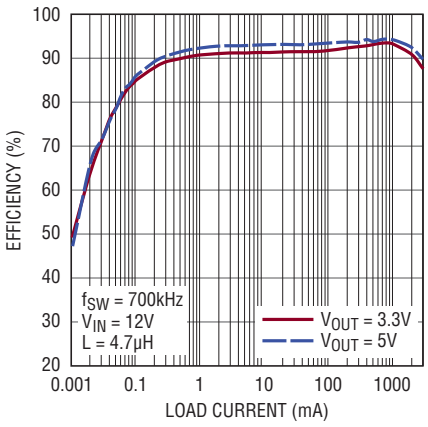
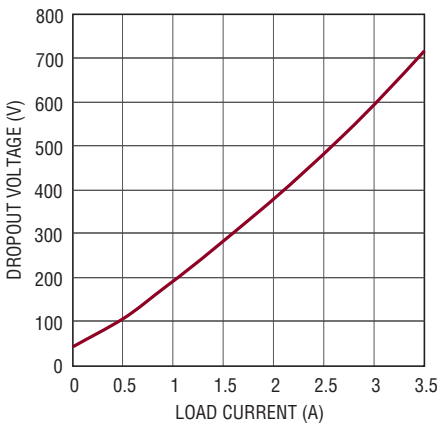
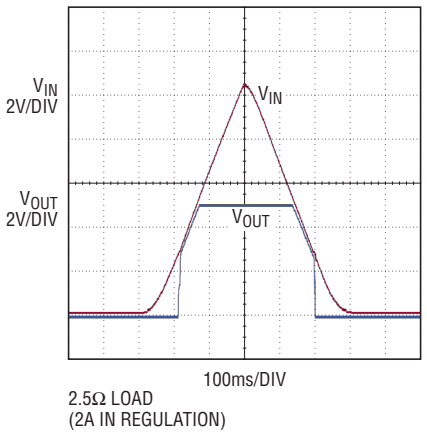


Figure 9. Efficiency for 3.3V and 5V outputs is above 90%, reducing total power dissipation and keeping temperature under control.



(a)



(b)

Figure 10. The LT8610AB operates to 99% duty cycle, providing smooth start-up and low dropout voltage.

Prioritize Power Sources in Any Order, Regardless of Relative Voltage: No µP Required

Sam Tran

Does your application have multiple input power sources? Are one or more secondary source voltages equal to or higher than the main source? How do you ensure the main source powers the output when a higher voltage, secondary source is present? How do you prevent sources from cross conducting, or backfeeding during input source switchover? Do you need to prevent current sharing between similar voltage sources? Are you worried about users plugging in sources backwards or plugging in overvoltage sources to the system? The LTC4417 prioritized PowerPath™ controller, with its wide 2.5V to 36V operating voltage range, solves all these issues by controlling the connection of the input sources based on user-defined priority and validity while protecting the system from overvoltage and reverse voltage insertions up to ±42V.

PRIORITIZING THREE INPUT SOURCES

Figure 1 shows a triple-input prioritizer. Here, the 12V wall adapter is given top priority, the 14.8V Li-ion battery stack is prioritized second, and 12V sealed lead acid (SLA) battery has the lowest priority. Priority is simply set by connecting the sources to the LTC4417 in pin order: V1 is the highest priority; V3 the lowest priority.

The LTC4417 connects a higher priority input source to the output as long as the input source voltage remains valid—i.e., within its resistive-divider-defined overvoltage (OV) and undervoltage (UV) window. As long as the higher priority source remains valid, lower priority inputs remain disconnected, regardless of their relative voltages.

Accurate (±1.5%) comparators continuously monitor each input's OV and UV pins to ensure an input source is stable for at least 256ms before validating and allowing a connection to the output. Input sources are quickly disconnected if an OV or

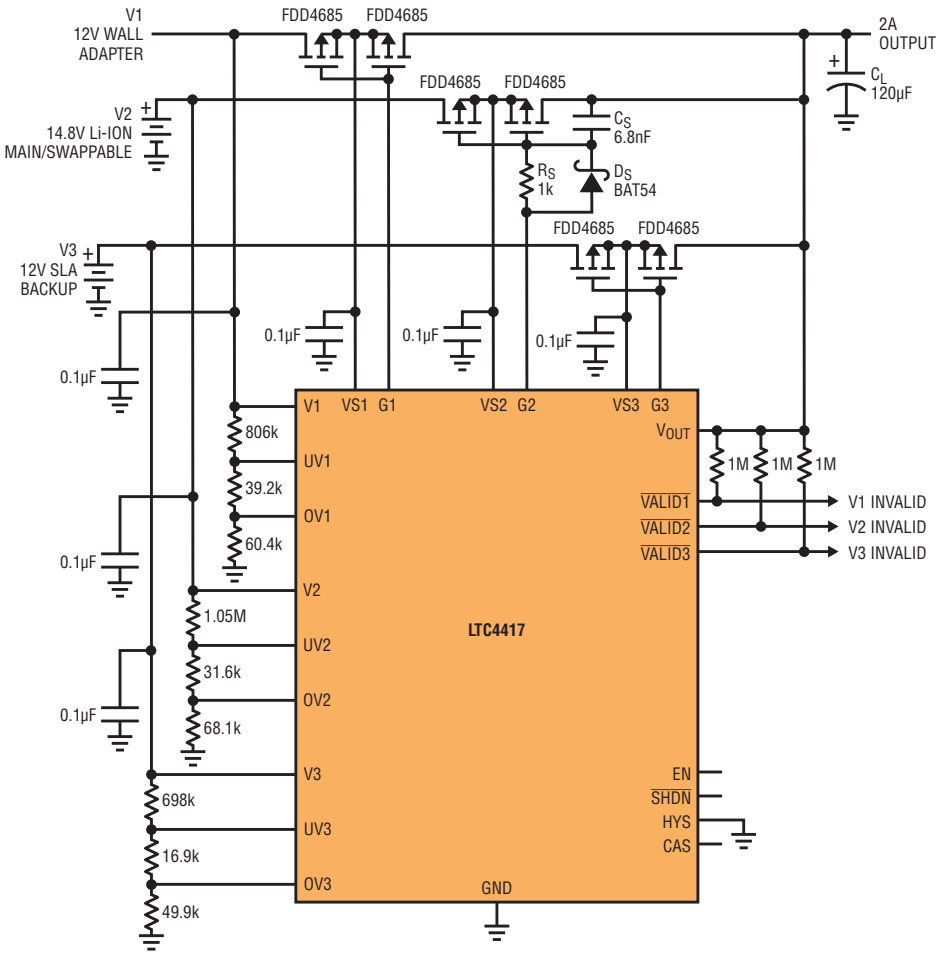


Figure 1. Triple input LTC4417 prioritized input source selection application

The high voltage (2.5V to 36V), triple input LTC4417 prioritized PowerPath controller is easy to use, robust and complete. Automatically prioritized supply current sourcing extends the life of lower priority input sources while controlled switching protects input sources from cross and reverse conduction during switchover.

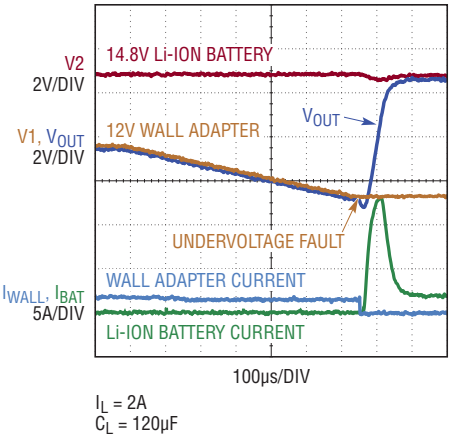


Figure 2. Switchover from a lower voltage input to a higher voltage input

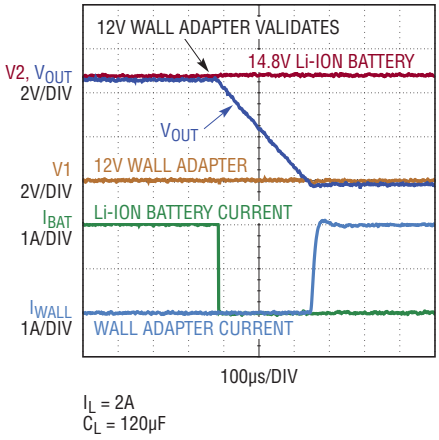


Figure 3. Switchover from a higher voltage to a lower voltage input

UV condition is sensed. An internal 8µs OV, UV filter time helps prevent false tripping.

Switching over to another valid input source can only occur when an OV or UV fault is detected or a higher priority source becomes valid. Referring again to Figure 1, this allows the lower voltage, higher priority 12V wall adapter to remain connected to the output provided it is valid. If another source is powering the output, the 12V wall adapter is reconnected to the output as soon as the wall adapter becomes valid.

The LTC4417 drives external back-to-back P-channel MOSFETs as switches to connect and disconnect input supplies to and from the output. Strong gate drivers ensure the back-to-back P-channel MOSFETs are firmly held off during input source insertion and provide enough strength to drive large, low $R_{DS(ON)}$, P-channel MOSFETs for reduced steady state power dissipation and increased output operating voltage range. An integrated 6.2V gate to source clamp prevents gate-to-source oxide overvoltage stress while allowing sufficient overdrive to enhance common logic level rated P-channel MOSFETs.

An important feature of the LTC4417 is the break-before-make circuit that protects input sources from cross-conduction during switchover. Gate-to-source (V_{GS}) comparators sense that the external MOSFETs of the disconnecting input source are off before another input source is allowed to connect to the common output. To prevent reverse conduction from the output to an input source during connection, reverse voltage (REV) comparators delay the connection if a higher output voltage is detected. Connection is delayed until the output voltage drops below the connecting input source voltage.

Figure 2 captures the event when the LTC4417 disconnects the 12V wall adapter from the output due to a UV fault. Once the V_{GS} comparator confirms that the disconnecting 12V wall adapter's back-to-back P-channel MOSFETs are off, the next highest priority valid input source, the 14.8V Li-ion battery, is immediately connected to the output. The two input source current waveforms show that no cross or reverse conduction occurs between the input sources during switchover, thanks to the V_{GS} comparator.

A resistor and capacitor, R_S and C_S in Figure 1, serve to limit the 14.8V Li-ion battery inrush current to a peak of 14A when it connects to the output. High inrush currents can cause input source UV faults, exceed the external MOSFET's maximum pulsed drain current (I_{DM}), or potentially damage connectors. The addition of R_S and C_S increases the switchover time, resulting in an output voltage droop of 400mV. Note that larger R_S and C_S values result in lower inrush currents at the expense of additional output voltage droop. Keep this trade-off in mind when selecting R_S and C_S. The Schottky diode, D_S, preserves the strong turn-off.

Figure 3 shows the LTC4417 disconnecting the lower priority valid 14.8V Li-ion battery stack to allow the newly validated higher priority 12V wall adapter to connect to the output. The REV comparator senses the initial 14.8V output voltage and prevents the 12V wall adapter from immediately connecting to the output. The REV comparator delays the connection until the output discharges below the 12V wall adapter voltage to ensure no reverse current occurs, as shown by the two input source current waveforms.

The LTC4417 drives external back-to-back P-channel MOSFETs as switches to connect and disconnect input supplies to and from the output. Strong gate drivers ensure the back-to-back P-channel MOSFETs are firmly held off during input source insertion and provide enough strength to drive large, low $R_{DS(ON)}$, P-channel MOSFETs for reduced steady state power dissipation and increased output operating voltage range.

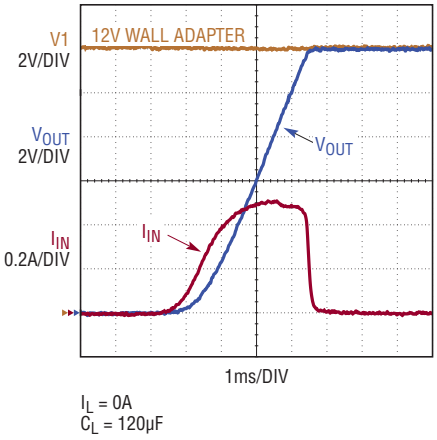


Figure 4. Output soft-start

Inrush current is also limited from the 12V wall adapter because it is quickly switched in when the output voltage is 11.88V. As its current waveform shows, the wall adapter provides the 2A load current plus the small additional current necessary to charge V_{OUT}.

PRIORITIZED, LOW I_{CC} MINIMIZES POWER DRAW

The LTC4417 draws only 28µA of total operating current, and it draws as much of this as possible from the highest priority valid supply. During normal operation, more than half the supply current is drawn from the output when V_{OUT} is above 2.5V. When V_{OUT} is less than 2.5V, operating current is drawn from the highest priority valid input supply, with any remaining supply current sourced from the highest voltage input source. The LTC4417 consumes almost no current from lower priority input sources when their voltages are lower than the output voltage.

When $\overline{SHDN}$ is forced low, the part is placed into a suspended mode where the OV and UV comparators are powered down to conserve power and all input sources are invalidated. In this state, the supply current is drawn from the highest voltage source.

OUTPUT SOFT-START

High inrush currents can occur when a higher voltage input source quickly connects to a lower voltage output bulk capacitor. When the output voltage is less than 0.7V, the LTC4417 soft starts V_{OUT} to minimize inrush current.

Figure 4 shows the input current and output voltage waveforms when the LTC4417 soft-starts from the 12V wall adapter to an initially discharged 120µF output bulk capacitor. As the figure shows, the peak input current is limited to 500mA.

After the output has been connected to its first supply, systems with similar voltages have minimal inrush current when changing channels due to the similar input and output voltages during input source switchover. This allows systems with similar input source voltages to omit the R_S, C_S, and D_S inrush current limiting circuitry shown in Figure 1.

Figure 5. 24V Application with reverse voltage protection

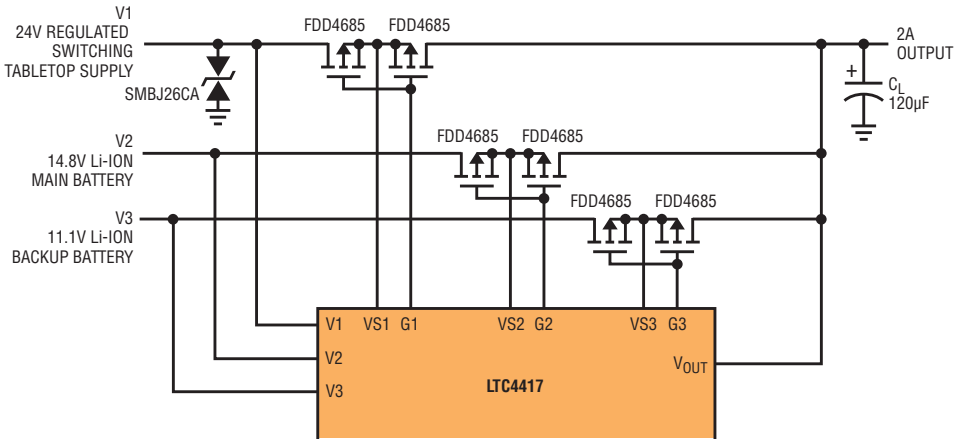
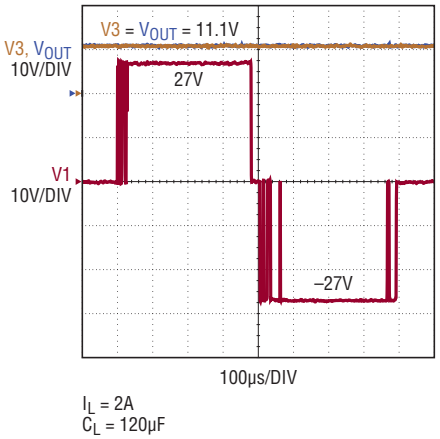


Figure 6. Over and reverse voltage blocking



With input source pins, V1 to V3, designed to handle ±42V, the LTC4417 only requires that the external P-channel MOSFETs be chosen with a BV_{DSS} rating greater than any anticipated voltage excursions from input to output for seamless over, under and reverse voltage input source insertion protection.

OVERVOLTAGE, UNDERVOLTAGE AND REVERSE VOLTAGE INSERTION PROTECTION

Applications where sources are physically plugged in and unplugged face the possibility of improper or faulty source insertions. Faulty wall adapter insertions can expose the system to potentially damaging overvoltage events while reverse voltage insertion can occur from improperly inserted batteries. These miscues can be compounded by the prevalence of standardized connectors with differing voltage specifications. With input source pins, V1 to V3, designed to handle ±42V, the LTC4417 only requires that the external P-channel MOSFETs be chosen with a BV_{DSS} rating greater than any anticipated voltage excursions from input to output for seamless over, under and reverse voltage input source insertion protection.

Figure 5 shows a complete input fault insertion protected system. The LTC4417 protects itself against input voltage ranging from –42V to 42V. The –40V BV_{DSS} FDD4685 P-channel MOSFETs are chosen to withstand the worst-case voltage excursion. During insertion, a 256ms deglitch timer ensures the strong gate drivers initially hold the external MOSFETs off. Transient voltage suppressor (TVS) diodes, highly recommended with input voltages above 20V, ensure transient voltage excursions do not exceed the LTC4417's absolute maximum voltage of ±42V. Figure 6 shows the LTC4417 blocking a forced V1 overvoltage step of 27V and subsequent –27V reverse voltage step from the 11.1V Li-ion battery stack and output. Inrush current limiting circuitry is not shown in Figure 5 for simplicity.

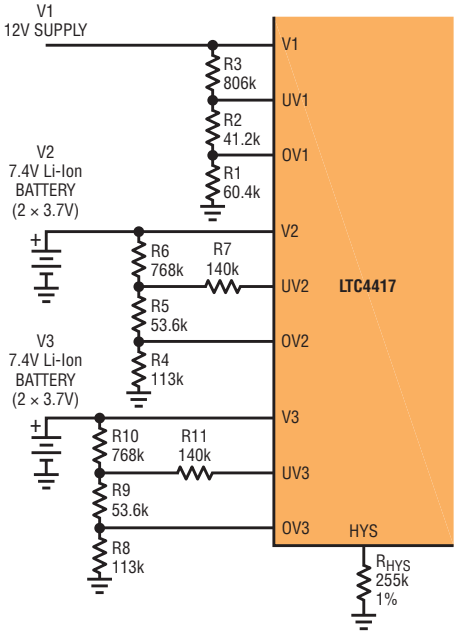


Figure 7. Configuring hysteresis voltages

HIGH IMPEDANCE INPUT SOURCE APPLICATIONS

Internal series resistance, present in all batteries and capacitors, produces a voltage drop that lowers the operating voltage when load currents are present. Removal of the load current allows the voltage source to recover this voltage drop. Some batteries and capacitors can recover hundreds of millivolts when load currents are disconnected due to a UV fault. If insufficient hysteresis is provided, the input source can reenter its valid window and reconnect.

For these situations, the LTC4417 allows the user to enable and set a hysteresis current through an external resistor, R_{HYS}. When hysteresis is switched in, one-eighth of the current flowing through R_{HYS} flows through the OV, UV resistive dividers to generate the hysteresis voltage. By adjusting the value of the resistive dividers and/or adding a resistor in series with the OV and UV pins, individual hysteresis voltages can be tailored to each input source's internal resistance characteristic, preventing false reconnection after recovery.

Figure 7 shows a 255kΩ resistor, R_{HYS}, setting 245nA of hysteresis current through the resistive dividers, R1 through R3, to generate approximately 200mV of OV and UV hysteresis at the 12V wall adapter. Resistive T-structures, R4 through R7 and R8 through R11, are used to set independent OV and

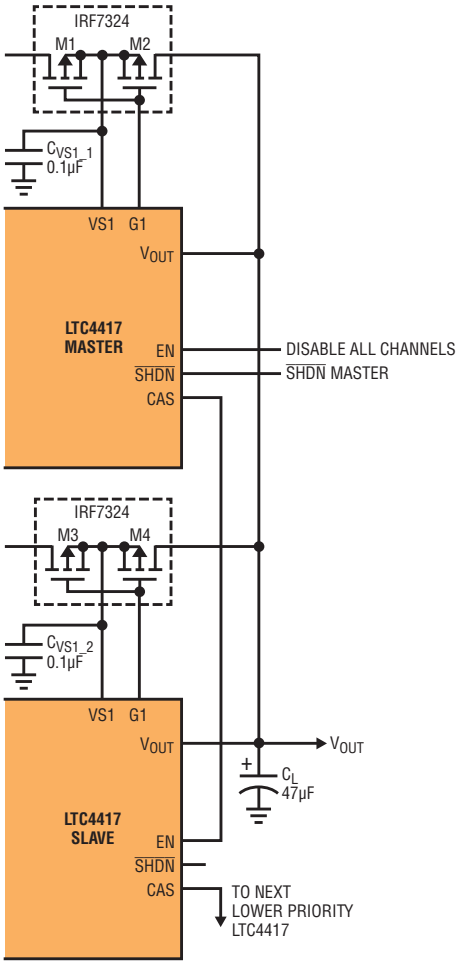
The LTC4417 can easily be cascaded to prioritize any number of input sources. Simply connect all of the cascaded LTC4417s' V_{OUT} pins to the system output and connect any higher priority LTC4417 CAS pin to the next lower priority LTC4417 EN pin.

UV hysteresis voltages of 201mV and 390mV, respectively, at the Li-ion batteries.

PRIORITIZE ANY NUMBER OF SOURCES

The LTC4417 can easily be cascaded to prioritize any number of input sources. Simply connect all of the cascaded LTC4417s' V_{OUT} pins to the system output and connect any higher priority LTC4417 CAS pin to the next lower priority LTC4417 EN pin as shown for two LTC4417s in Figure 8. Additional LTC4417 can be cascaded by daisy-chain connecting their CAS and EN pins. Driving the highest priority LTC4417 EN pin low disconnects all input sources from the common output. Driving the highest priority LTC4417 $\overline{SHDN}$ pin low disables that LTC4417 and allows the next LTC4417 in the serial chain to control the output.

Figure 8. Cascading application



CONCLUSION

The high voltage (2.5V to 36V), triple input LTC4417 prioritized PowerPath controller is easy to use, robust, and automously allows applications to be powered from a variety of input sources, independent of voltage. Automatically prioritized supply current sourcing extends the life of lower priority input sources while controlled switching protects input sources from cross and reverse conduction during switchover.

Key features such as continuous input source monitoring through ±1.5% accurate overvoltage and undervoltage comparators, 256ms input deglitch time, and strong gate drivers with an integrated 6.2V clamp, enable overvoltage, undervoltage, and reverse voltage protection from faulty input source connections.

Resistive divider defined overvoltage and undervoltage trip points, adjustable current mode hysteresis, external inrush current limiting, and external back-to-back P-channel MOSFETs make the LTC4417 customizable to numerous applications. The LTC4417 is available in 24-lead GN and leadless 4mm × 4mm QFN packages. Both packages are available in C, I and –40°C to 125°C H grades.

Visit www.linear.com/LTC4417 for data sheets, demo boards and other applications information. ■

3mm × 3mm QFN IC Directly Monitors 0V to 80V Supplies: Features I²C Interface, Peak Value Tracking and Runs from Any Supply

CY Lai

Power monitoring in combination with control mechanisms can significantly boost system energy efficiency and reliability. The LTC2945 is a highly integrated digital power monitoring solution that is compact, rugged and easy-to-use. It is designed to fit applications requiring power monitoring with a minimal number of components.

Figure 1 shows the LTC2945's functional block diagram. All basic elements required for power monitoring are integrated, including a precision current sense amplifier, precision resistive dividers, an analog-to-digital converter (ADC) and an I²C interface for communicating with the host controller. Only an external current sense resistor is required. The host can periodically poll the LTC2945 for available power data, minimum and maximum values are stored, and an alert can be sent from the LTC2945 to interrupt the host when measured values exceed their preprogrammed limits.

MONITOR POWER ON ANY SUPPLY

The LTC2945's internal current sense amplifier features a common mode range of 0V to 80V to suit a wide variety of high side and low side current sensing applications. Most wide range supply monitors available today require a low voltage secondary supply for operation, which can be undesirable for several reasons:

- There is no suitable secondary supply
- The secondary supply, often loaded with noisy digital circuits, must be sufficiently filtered or bypassed due to the finite power supply rejection ratio of the supply monitor at higher frequencies
- The secondary supply exists, but is not readily accessible—it is inconveniently located on the printed circuit board, complicating the routing of a power line

The LTC2945 avoids these problems by integrating a high voltage linear regulator that can be powered directly from 4V to 80V supplies. The output of the linear regulator ($INTV_{CC}$) powers the LTC2945, and can be externally bypassed to prevent supply noise from corrupting the signal integrity of internal circuitry. The linear regulator is capable of supplying a 10mA load, saving the cost of a dedicated high voltage linear regulator needed to power circuits such as opto-couplers in some applications.

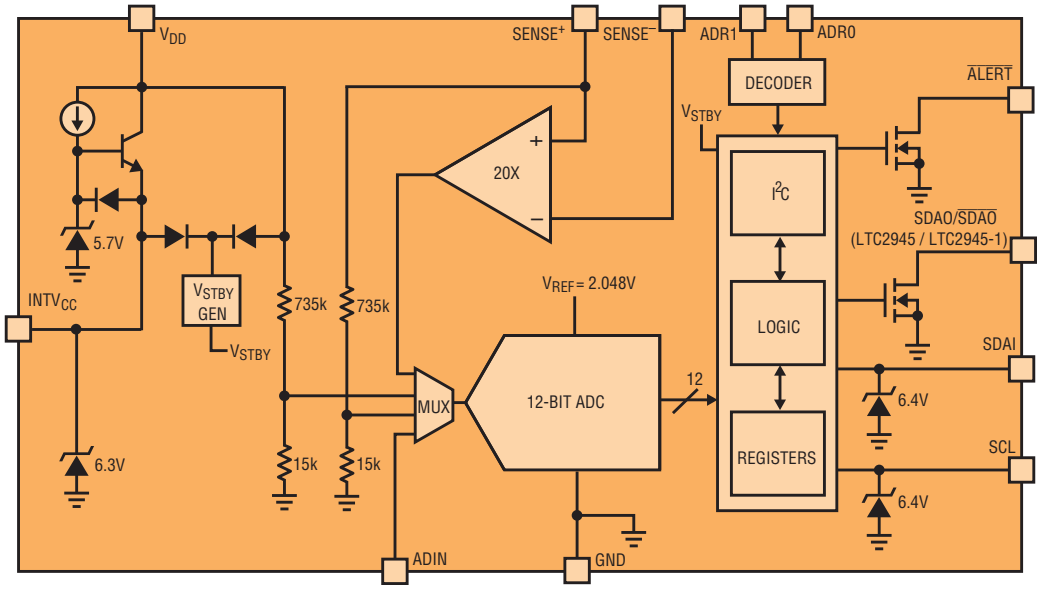


Figure 1. Functional block diagram of the LTC2945

The LTC2945 is a highly integrated power monitor that easily fits into a wide range of systems. It offers a 0V to 80V common mode range, 2.7V to 80V operating range, ±0.75% accurate voltage and current measurements, and an on-chip digital multiplier that computes power.

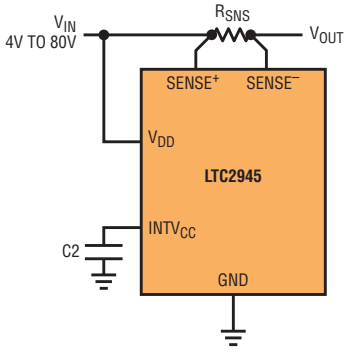


Figure 2a. The LTC2945 deriving power from the monitored supply

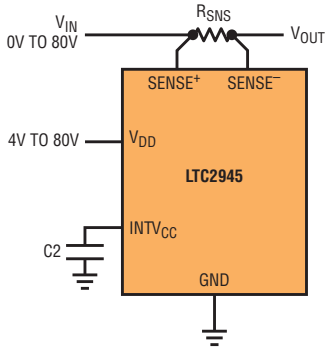


Figure 2b. The LTC2945 deriving power from a wide ranging secondary supply

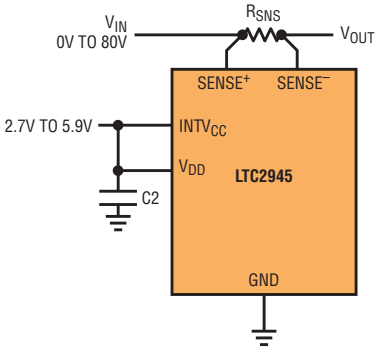


Figure 2c. The LTC2945 deriving power from a low voltage secondary supply

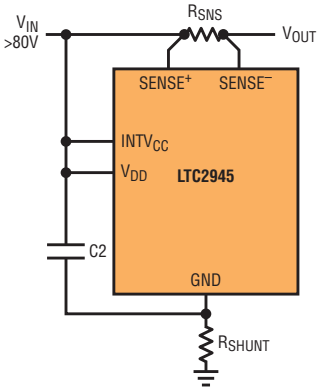


Figure 3a. The LTC2945 deriving power through a high side shunt regulator

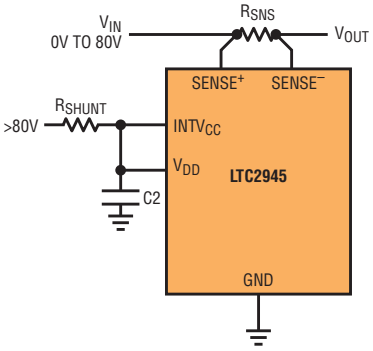


Figure 3b. The LTC2945 deriving power through a low side shunt regulator in a high side current sense topology

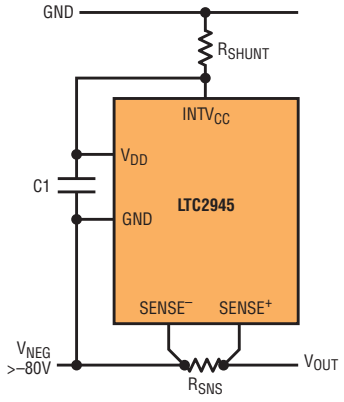


Figure 3c. The LTC2945 deriving power through a low side shunt regulator in a low side current sense topology

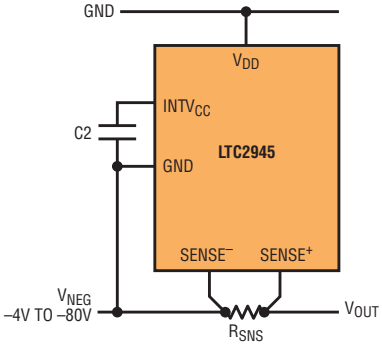


Figure 3d. The LTC2945 deriving power from the monitored supply in a low side current sense topology

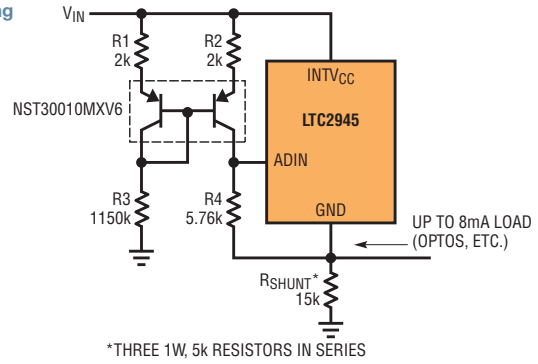
Figure 2a shows a typical LTC2945 application monitoring a 4V to 80V supply and deriving power off the same supply. The bus voltage is measured at the SENSE+ pin through an internal resistive divider and a sense resistor is used to measure the load current on the high side. If the bus voltage to be monitored is below 2.7V, the power for the LTC2945 can be derived from a wide range secondary supply as shown in Figure 2b or a low voltage secondary supply as shown in Figure 2c.

The LTC2945 also integrates a 6.3V, 35mA shunt regulator at the $INTV_{CC}$ pin for operation beyond 80V. Figure 3a shows the LTC2945 used in one such application with its ground floated at 6.3V below the bus voltage. The bulk of the bus voltage is dropped across an external shunt resistor; in practice any current source capable of standing off the bus voltage and supplying LTC2945's operating current will work.

Figure 4 shows how to measure the bus voltage in this configuration using a matched PNP pair and some resistors. The resistor values shown are optimized for V_{IN} of 165V ±10%. The LTC2945's shunt regulator can also be configured as shown in Figure 3b when the only

LTC2945 integrates an oversampling ΔΣ ADC that inherently averages the measured voltage over the conversion cycle to effectively reject noise due to transient spikes and AC power line. Bus voltage, sense voltage and ADIN are measured with total error of less than ±0.75% at full scale over the full industrial temperature range.

Figure 4. Application circuit for measuring the bus voltage in a high side shunt regulator configuration



secondary supply available exceeds 80V in high side current sensing applications.

If the output of the power supply is negative such as in –48V distributed power systems for networking, communications and high end computing equipment, low side current sensing is generally preferred, as shown in Figures 3c and 3d. Figure 3c shows a shunt resistor and LTC2945's shunt regulator limiting $INTV_{CC}$ to 6.3V above a negative supply that exceeds 80V. More commonly, the negative supply is below 80V and instead the internal linear regulator can be used to power the LTC2945 directly, as shown in Figure 3d. In this configuration the V_{DD} pin measures the bus voltage through an internal resistive divider.

Measuring bus voltage in excess of 80V in low side current sensing applications such as Figure 3c can be done by connecting a resistive divider to the ADIN pin as shown in Figure 5.

±0.75% TOTAL ERROR MEASUREMENT ACCURACY

LTC2945 integrates an oversampling ΔΣ ADC that inherently averages the measured voltage over the conversion cycle to effectively reject noise due to transient spikes and AC power line harmonics. Bus voltage, sense voltage and ADIN are measured with total error of less than ±0.75% at full scale over the full industrial temperature range.

The 12-bit ΔΣ ADC provides a full-scale voltage of 102.4mV (25µV/LSB) for sense voltage, 102.4V (25mV/LSB) for bus voltage and 2.048V (0.5mV/LSB) for ADIN. Typical integral linearity error (INL) of the ADIN voltage and the sense voltage are both well within ±0.5LSB, as shown in Figures 6 and 7. The LTC2945 is also ideal in applications where accuracy is important at the low end of the measurements since its specified offset voltages are as low as ±1.1LSB for ADIN and ±3.1LSB for current sense voltage in the worst case.

Figure 5. ADIN senses the bus voltage in low side shunt regulator configuration.

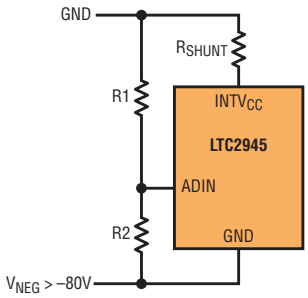


Figure 6. ADIN INL curve

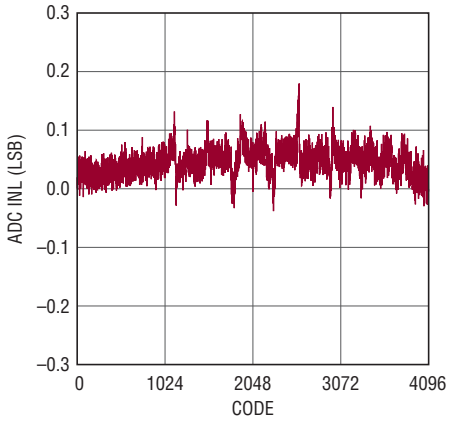
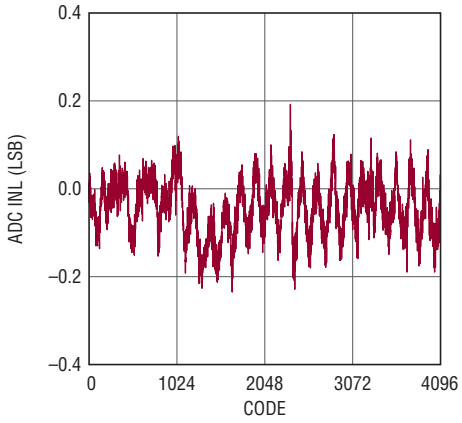


Figure 7. SENSE INL curve



Opto-isolation is common in high voltage systems where the high voltage sections must be galvanically isolated for safety reasons. The LTC2945 accommodates isolated applications by splitting the SDA signal on the I²C interface into an SDAI pin and an SDAO pin (for LTC2945-1, $\overline{\text{SDAO}}$) for applications with an opto-isolator interface.

PEAK VALUES TRACKING AND OVER/UNDERVALUE ALERTS

Keeping track of the minimum and maximum measurement values is important in many power monitoring systems because it could be used to study usage behavior for more efficient resource allocation and is often an indicator of system health. Previously, gathering such information required periodic polling of the power monitor by the system's microprocessor, which wasted precious computation time and potentially tied up the I²C interface. The LTC2945 solves this problem by storing the minimum and maximum values for power, voltage, current, and ADIN. The Page Read feature on the LTC2945 allows these data to be read with just a single I²C read transaction. An $\overline{\text{ALERT}}$ pin can also be configured to signal overvalue or undervalue limit violations for power, voltage, current and ADIN.

UNTRUNCATED 24-BIT POWER DATA

For applications where a digital servo loop is used to regulate the power output of a system, the power data read back from the monitor needs to be monotonic and of high resolution in order to minimize stability issues. The LTC2945 generates 24-bit power data by digitally multiplying the 12-bit sense voltage and 12-bit bus voltage data without truncating the result.

OPTO-ISOLATION AND SHUTDOWN

The LTC2945 can be shut down via the serial I²C interface, reducing the typical quiescent current to 20µA—especially important for battery-powered applications. Opto-isolation is common in high voltage systems where the high voltage sections must be galvanically isolated for safety reasons. The LTC2945 accommodates isolated applications by splitting the SDA signal on the I²C interface into an SDAI pin and an SDAO pin (for LTC2945-1, $\overline{\text{SDAO}}$) for applications with an opto-isolator interface as shown in Figure 8.

For limited amounts of current, the internal linear regulator or shunt regulator can be used to supply the pull-up resistors on the I²C bus. In situations where it is undesirable to tap off the internal regulator and a low voltage supply is not available, the LTC2945-1 allows the pull-up resistors to connect directly to high voltages. The SCL and the SDAI pins are limited to safe voltages by internal 6.3V, 3mA clamps. The SDAO pin is inverted (to $\overline{\text{SDAO}}$) so that it can be clamped by the anode of the input diode of an optoisolator as shown in Figure 9.

SUPPLY TRANSIENTS

The wide operating range of the LTC2945 is advantageous even in applications where the bus voltage is normally well below 80V. Transient voltage surges due to inductive kickbacks in automotive load dump situations and hot swap output shorts are just two possible scenarios where a rugged power monitoring solution is required in order to withstand overvoltage conditions far in excess of the normal operating voltage.

The 100V absolute maximum rating of the LTC2945 makes it easy to guard against these types of voltage surges since there is a wide range of transient surge suppressor (TVS) diodes from which to choose. In certain applications a large

Figure 8. Opto-isolation of a 10kHz I²C interface between the LTC2945 and a microcontroller

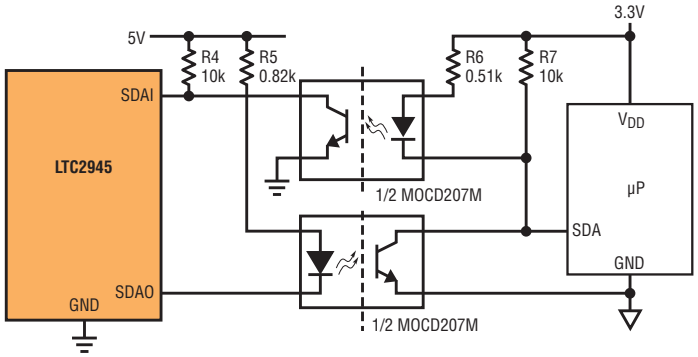
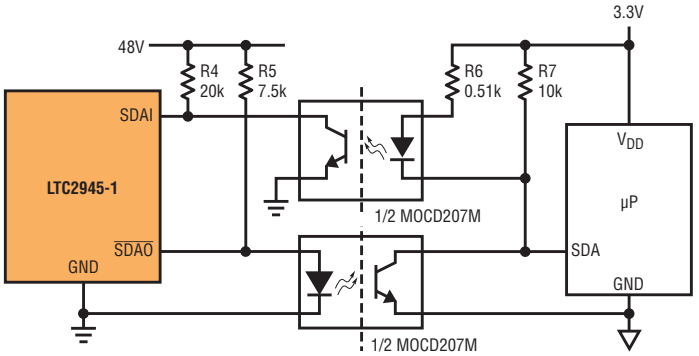


Figure 9 Opto-isolation of a 1.5kHz I²C interface between the LTC2945-1 and a microcontroller



The 100V absolute maximum rating of the LTC2945 makes it easy to guard against voltage surges since there is a wide range of transient surge suppressor (TVS) diodes from which to choose. In certain applications a large MOSFET power device can break down to clip the inductive spike safely, and in most 12V and 24V systems the break-down voltage of these power devices is less than 100V, potentially negating the requirement for a TVS diode.

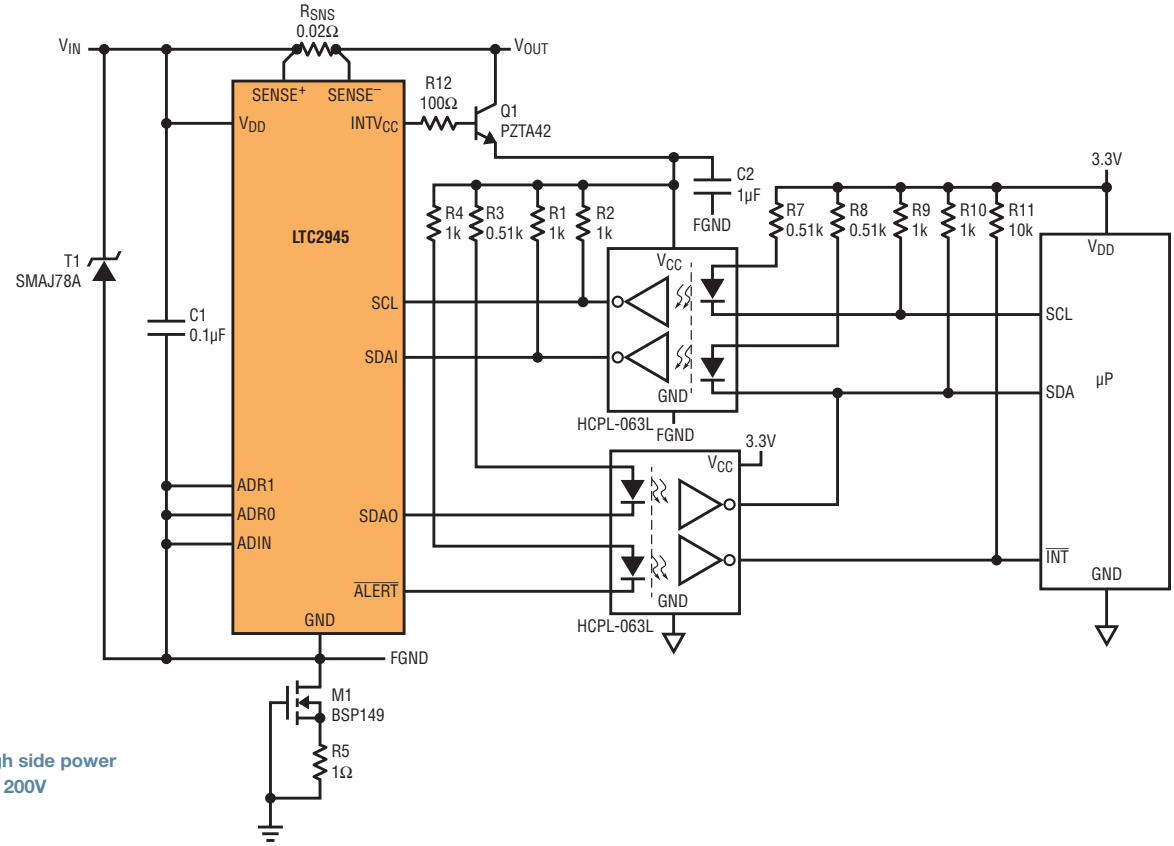


Figure 10. Ruggedized 4V to 80V high side power monitor with surge protection up to 200V

MOSFET power device can break down to clip the inductive spike safely, and in most 12V and 24V systems the break-down voltage of these power devices is less than 100V, potentially negating the requirement for a TVS diode.

Hard-clamping the voltage with TVS diode or MOSFET break down may not be practical when the inductive energy is too high or unpredictable. Figure 10 shows a LTC2945-based power monitor that can ride through a 200V surge where its high voltage pins are clamped by T1 to less than 80V. In normal operation, M1 operates in the triode region with the device ground at a few mV above the system ground. During the surge, the device ground is lifted by T1 and the balance of the surge voltage is dropped across M1. The BSP149 has a 200V break down and the surge duration is limited by its safe operating area—for example at room temperature it can survive a 200V surge for 1ms at V_{IN}.

CONCLUSION

The LTC2945 is a highly integrated power monitor that easily fits into a wide range of systems. It offers a 0V to 80V common mode range, 2.7V to 80V operating range, ±0.75% accurate voltage and current measurements, and an on-chip digital multiplier that computes power. Digital watchdog functions such as peak and valley values and window comparators are available for power, voltage, current and an external voltage. Opto-isolation is simplified with a split SDA pin. The LTC2945 is available in space-saving 3mm × 3mm QFN and 12-pin MSOP packages.

Visit www.linear.com/LTC2945 for data sheets, demo boards and other applications information. ■

High Efficiency Switching Power Conversion Combined with Low Noise Linear Regulation in µModule Package

David Ng

Devices with high speed or high resolution functions require clean power. Switching regulators offer efficiency across a variety of input/output conditions, but the typical switcher is hard pressed to deliver the clean, low output noise and fast transient response needed by high data rate FPGA I/O channels or high bit count data converters. In contrast, high performance linear regulators feature low output noise and fast transient response, but can quickly heat up.

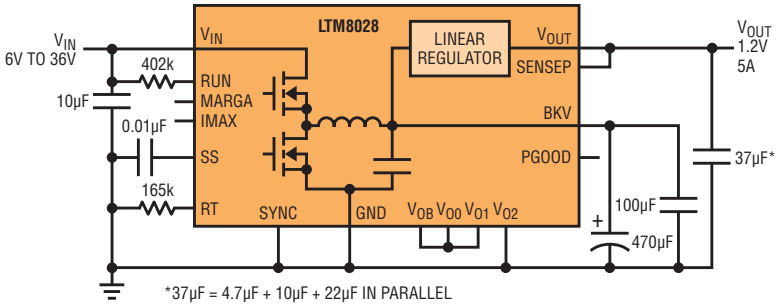


Figure 1. The LTM8028 is a 36V input, UltraFast, low output noise 5A µModule regulator.

The LTM®8028 combines the best of both worlds—a high efficiency synchronous switching converter controlled by an UltraFast™ linear regulator, both integrated into a small, 15mm × 15mm µModule® package. It is available in LGA (4.32mm tall) and BGA (4.92mm tall) lead styles, both of which are RoHS compliant.

The linear regulator controls the output of the switcher to 300mV above the desired output voltage to provide the optimum combination of headroom, efficiency and transient response. The LTM8028 accepts inputs as high as 40V and produces output voltages between 0.8V and 1.8V at up to 5A. A typical 1.2V output application is shown in Figure 1.

Figure 2. In a 12V input to 1.2V output, 5A application, the LTM8028 dissipates less than 4W and heats up by only 45°C.

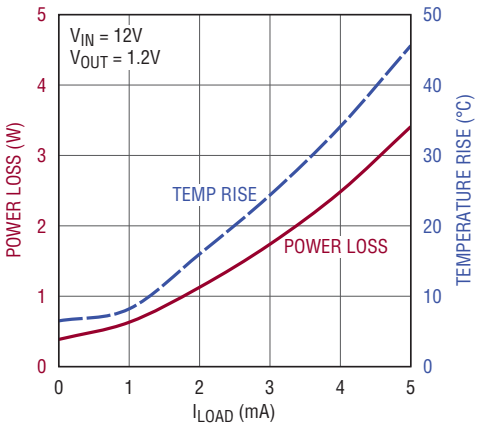


Figure 3. At 1.0V output, the LTM8028 transient response is less than 20mV.

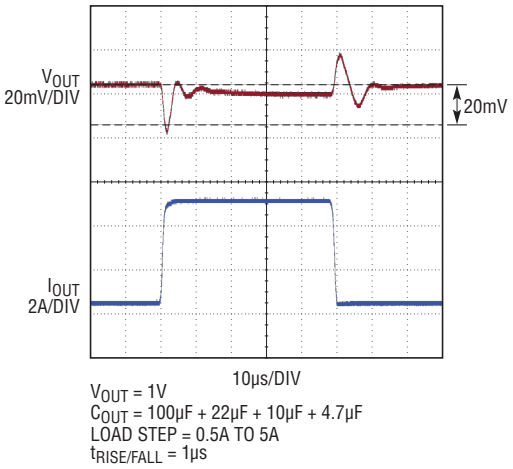
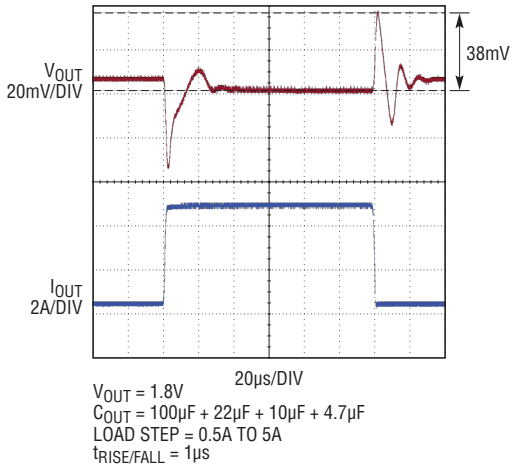


Figure 4. The LTM8028 transient response is only 38mV.



The linear regulator controls the output of the switcher to 300mV above the desired output voltage to provide the optimum combination of headroom, efficiency and transient response. The LTM8028 accepts inputs as high as 40V and produces output voltages between 0.8V and 1.8V at up to 5A.

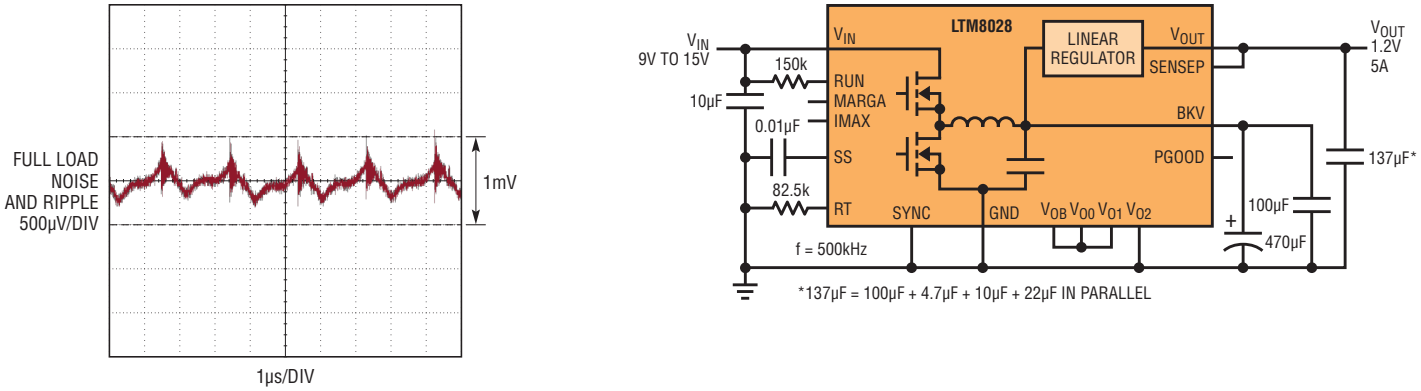
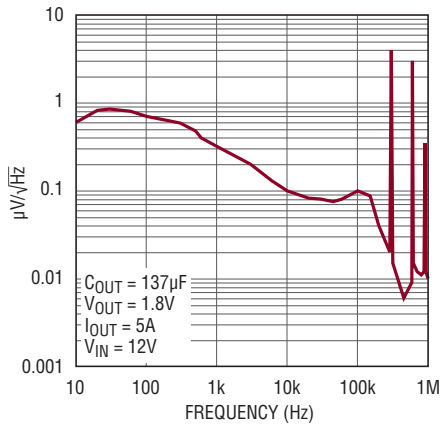


Figure 5. The peak-to-peak switching noise at the output of the LTM8028 is less than 1mV. (Schematic shows the setup used to achieve these results.)

The output voltage of the LTM8028 is set by controlling three 3-state inputs, V_{O0}, V_{O1} and V_{O2}. Applying a voltage to the MARGA pin allows the user to margin the output by as much as ±10%. The current limit may be reduced from the 5A maximum through the IMAX pin, and a PGOOD signal indicates that the output is within 10% of the target voltage.

Figure 6. The output noise spectral density, peaking at only 4µV/√Hz, makes the LTM8028 a good candidate for sensitive data conversion circuits.



A design using a traditional linear regulator providing 1.2V at 5A from a 12V source would burn over 50W and might require expensive heat sinking. The LTM8028, as shown in Figure 2, dissipates a twelfth of that, less at 4W, yielding a typical junction temperature rise of only 45°C.

The heart of the LTM8028 is the high performance linear regulator. Its total line and load regulation below 0.2% at room temp and 1% over its full –40°C to 125°C temperature range. Its UltraFast bandwidth gives the LTM8028 a 10%–90% load step transient response of only 2%. Figures 3 and 4 show the transient response of the LTM8028 when the load steps from 0.5A to 5A at a slew rate of 1A/µs when the device is configured to deliver 1V and 1.8V, respectively.

Even though the linear regulator and the synchronous switching converter are packaged together, high power supply rejection and integrated noise mitigation result in low output noise. Figure 5 shows peak-to-peak noise less than 1mV.[1]

In the frequency domain, the spectral noise content is very low, peaking at 4µV/√Hz at the switching converter's fundamental frequency of 300kHz as shown in Figure 6. This is important when powering high bit count data conversion circuits.

CONCLUSION

When a system design requires low power loss, tight regulation, fast transient response, and low output noise, reach for the LTM8028 µModule regulator. It combines the best features of high performance switching and linear regulators into a single, space efficient package.

Visit www.linear.com/LTM8028 for data sheets, demo boards and other applications information. ■

Notes

1 Measuring low amplitude noise can be tricky. This measurement was made using coaxial cables, impedance matching and a 150MHz HP461A amplifier. This is similar to the setup described in *Linear Technology Application Note 70*, "A Monolithic Switching Regulator with 100µV Output Noise" by Jim Williams, except the measurement here is not bandwidth limited to 10MHz.

µModule Regulator Powers and Protects Low Voltage µProcessors, ASICs and FPGAs from Intermediate Bus Voltage Surges

Willie Chan and Jason Sekanina

Intermediate bus voltages of 24V~28V nominal are commonplace in industrial, aerospace and defense systems where series-connected batteries may be a backup power source and 12V bus architectures tend to be impractical due to distribution losses. The widening voltage gap between the system bus and the power inputs of digital processors present design challenges relating to power delivery, safety and solution size.

If a single-stage non-isolated step-down DC/DC converter is used at the point of load, it must operate with extremely accurate PFM/PWM timing. Input surge events can stress DC/DC converters, presenting an overvoltage risk to the load. Erroneous or counterfeit capacitors introduced in manufacturing may cause output voltage excursions exceeding the load's ratings potentially causing the FPGA, ASIC or microprocessor to ignite. Depending on the extent of the damage, the root cause may be difficult to find.

An overvoltage risk mitigation plan is absolutely necessary to prevent customer dissastifaction. Traditional overvoltage protection schemes involving a fuse are not necessarily fast enough, nor dependable enough, to protect modern FPGAs, ASICs and microprocessors, particularly when the upstream voltage rail is 24V or 28V nominal. Active protection at the POL DC/DC is necessary. The LTM4641 is a 38V-rated, 10A DC/DC step-down µModule® regulator that defends against, and recovers from, many faults, including output overvoltage.

IMPORTANCE OF ACCURATE SWITCHER TIMING INCREASES WITH INPUT VOLTAGE & SURGES

When a wide differential exists between the input and the output voltages, switching DC/DC regulators are favored over linear regulators for their much higher efficiency. To achieve a small solution size, a nonisolated step-down converter is the top choice, operating at high enough frequency to shrink the size requirements of its power magnetics and filter capacitors.

However, in high step-down ratio applications, a DC/DC switching converter must operate at duty-cycles down to 3%, demanding accurate PWM/PFM timing. Furthermore, tight voltage regulation is required by digital processors, and fast transient response is needed to keep the voltage within safe limits. At relatively high input voltages, the margin for error in the on-time of the top side switch of the DC/DC regulator is reduced.

Bus voltage surges, which are often present in aerospace and defense applications, pose a danger not only to the DC/DC converter, but also to the load. The DC/DC converter must be rated to regulate through the overvoltage surge with a fast control loop, so that sufficient line rejection is achieved.

If the DC/DC converter fails to regulate or survive a bus surge, an overvoltage is presented to the load. Overvoltage faults may also be introduced as the load's bypass capacitors degrade with age and temperature, which results in looser transient load response over the course of the end product's life. If the capacitors degrade beyond the limits of the control loop's design, the load can be exposed to overvoltage by two possible mechanisms:

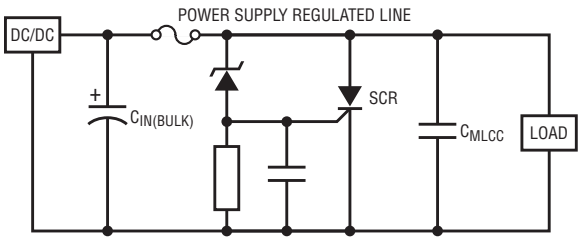


Figure 1. Traditional overvoltage protection circuit consisting of a fuse, SCR and Zener diode. While inexpensive, this circuit's response time is insufficient to reliably protect the latest digital circuits, particularly when the upstream supply rail is an intermediate voltage bus. Moreover, recovery from an overvoltage fault is invasive and time consuming.

The LTM4641 is a 38V-rated, 10A DC/DC step-down µModule switching regulator that defends against, and recovers from, many faults, including output overvoltage.

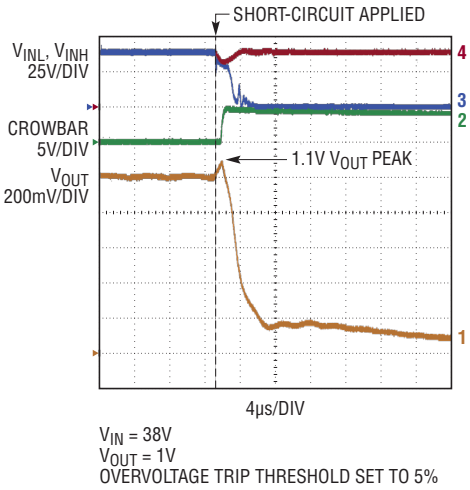


Figure 2. The LTM4641 responds to an overvoltage condition within 500ns, protecting the load from voltage stress.

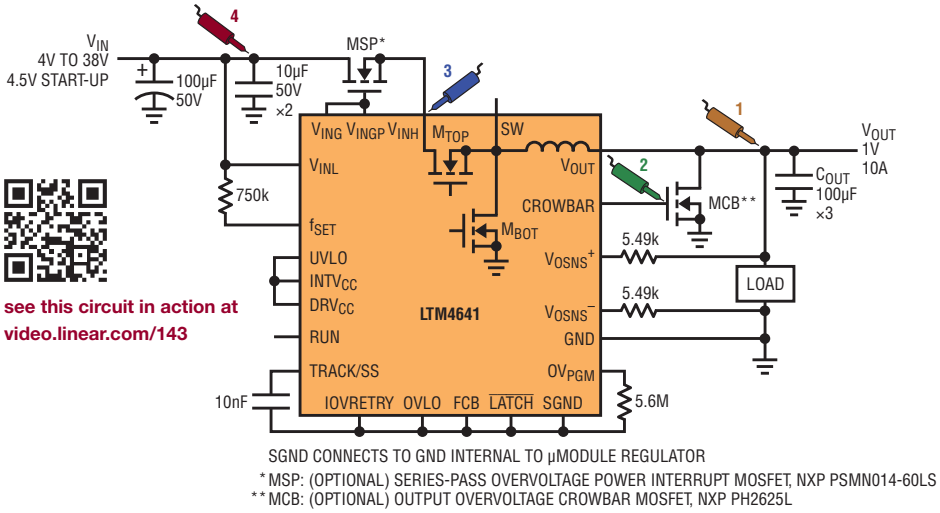


Figure 3. LTM4641 output overvoltage protection plan. The probe icons correspond to the waveforms in Figure 2.

- First, even if the control loop remains stable, heavy transient load-step events will demonstrate higher voltage excursions than were expected at the onset of design.
- Second, if the control loop becomes conditionally stable (or, worse yet, unstable), the output voltage can oscillate with peaks exceeding acceptable limits. Capacitors can also degrade unexpectedly or prematurely when an incorrect dielectric material is used, or when fake components enter the manufacturing flow.

CHEAP COUNTERFEIT COMPONENTS GENERATE EXPENSIVE HEADACHES

Gray market or black market counterfeit components can be enticing, but they don't meet the standards of the genuine article (e.g., they may be recycled, reclaimed from electronic waste, or built from inferior materials). A short-term savings becomes a huge long-term expense when a counterfeit product fails.

Counterfeit capacitors, for example, can fail in a number of ways. Counterfeit tantalum capacitors have been seen to suffer internal self-heating with a positive-feedback mechanism to the point of reaching thermal runaway. Counterfeit ceramic capacitors may contain compromised or inferior dielectric material, resulting in an accelerated loss of capacitance with age or at elevated operating temperatures. When capacitors fail catastrophically or degrade in value to induce control loop instability, the voltage waveforms can become much greater in amplitude than originally designed, endangering the load.

Unfortunately for the industry, counterfeit components are increasingly finding their way into the supply chain and electronics manufacturing flow, even in the most sensitive and secure applications. A United States Senate Armed Services Committee (SASC) report released publicly in May 2012 found widespread counterfeit electronic components in military aircraft and weapon systems that could compromise their performance and reliability—systems built by the top contractors in the defense industry. Coupled with the increasing number of electronic components in such systems—more than 3,500 integrated circuits in the new Joint Strike Fighter—counterfeit components pose a system performance and reliability risk that can no longer be ignored.

RISK MITIGATION PLANNING

Any risk mitigation plan should consider how the system would respond to and recover from an overvoltage condition. Is the possibility of smoke or fire resulting

see this circuit in action at video.linear.com/148

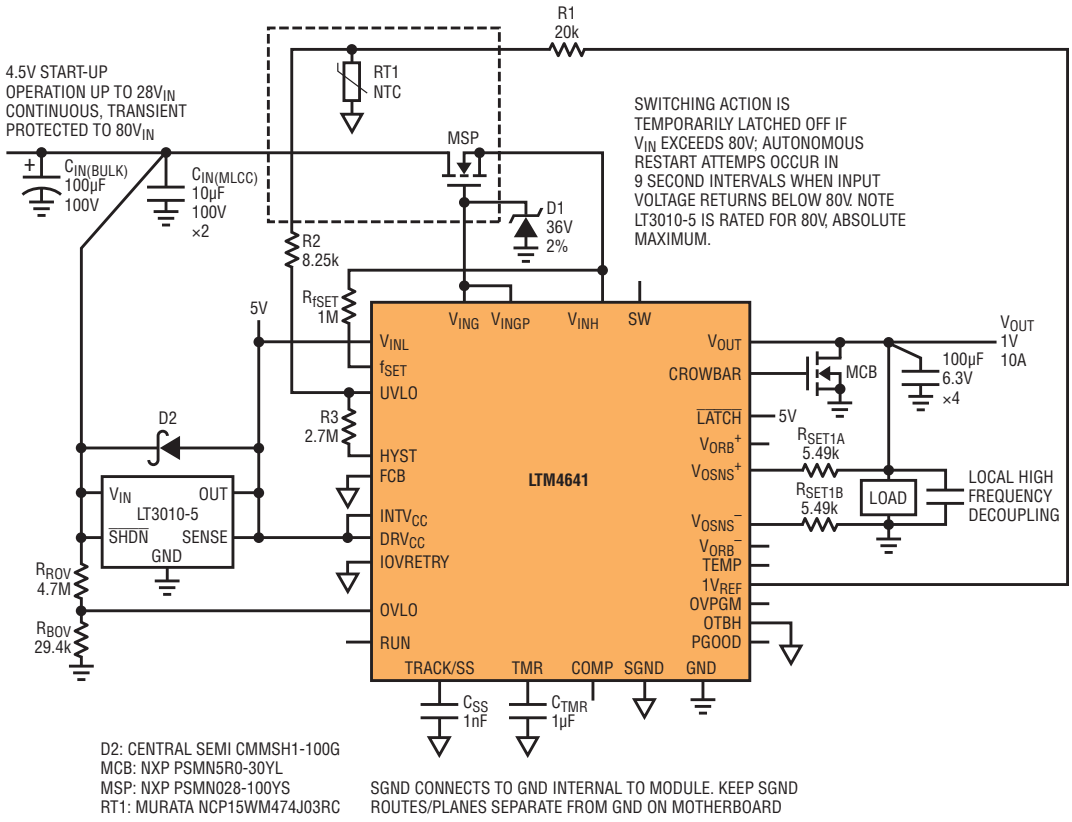


Figure 4. Input surge protection up to 80V, using the LTM4641 and an external LDO

from an overvoltage fault acceptable? Would efforts to determine root cause and implement corrective actions be hampered by damage resulting from an overvoltage fault? If a local operator were to power-cycle (reboot) a compromised system, would even greater harm to the system result further hindering recovery efforts? What is the process and time required to determine the cause of the fault and resume normal system operation?

INADEQUACIES OF TRADITIONAL PROTECTION CIRCUIT

A traditional overvoltage protection scheme consists of a fuse, silicon controlled rectifier (SCR), and Zener diode (Figure 1). If the input supply voltage exceeds the Zener breakdown voltage, the SCR activates, drawing sufficient current to blow open the upstream fuse.

This straightforward circuit is relatively simple and inexpensive, but there are drawbacks of this approach:

- Variations in the Zener diode breakdown voltage, SCR gate trigger threshold, and current required to blow the fuse result in inconsistent response times. Protection may engage too late to prevent hazardous voltage from reaching the load.
- The level of effort required to recover from a fault is high, involving physically servicing the fuse and restarting the system.
- If the voltage rail under consideration powers the digital core, an SCR's protection capability is limited, since the forward drop at high currents is comparable to or above the core voltage of the latest digital processors.

Because of these drawbacks, the traditional overvoltage protection scheme is not suitable for high voltage to low voltage DC/DC conversion powering loads such as ASICs or FPGAs that could be valued in the hundreds if not thousands of dollars.

COMBINE POWER AND FAULT PROTECTION FOR FAST AND DEPENDABLE REACTION AND RECOVERY

A better solution would be to accurately detect an imminent overvoltage condition and respond by quickly disconnecting the input supply while discharging excess voltage at the load with a low impedance path. This is possible with the protection features in the LTM4641.

At the heart of the device is a 38V-rated, 10A step-down regulator with the inductor, control IC, power switches and compensation all contained in one surface mount package. It also includes extensive monitoring and protection circuitry to protect high value loads such as ASICs, FPGAs and microprocessors. The LTM4641 maintains a constant watch for input undervoltage, input overvoltage, overtemperature and output overvoltage and overcurrent conditions and acts appropriately to protect the load.

Overvoltage protection in mission critical systems must be fast, accurate and consistent—at levels beyond the capabilities of the traditional SCR/fuse-based scheme. The LTM4641 combines an efficient 10A DC/DC step-down regulator with a fast and accurate output overvoltage protection circuit in one surface mount package to meet demanding protection requirements.

To avoid false or premature execution of the protection features, each of these monitored parameters has built-in glitch immunity and user adjustable trigger thresholds with the exception of overcurrent protection, which is implemented reliably, cycle-by-cycle with current-mode control. In the case of an output overvoltage condition, the LTM4641 reacts within 500ns of fault detection (Figure 2).

The LTM4641 responds nimbly and reliably to protect downstream devices, and, unlike fuse-based solutions, it can automatically reset and rearm itself after fault conditions have subsided. The LTM4641 uses an internal differential sense amplifier to regulate the voltage at the load's power terminals, minimizing errors stemming from common-mode noise and PCB trace voltage drops between the LTM4641 and the load. The DC voltage at the load is regulated to better than ±1.5% accuracy over line, load and temperature. This accurate output voltage measurement is also fed to the fast output overvoltage comparator, which triggers the LTM4641's protection features.

When an overvoltage condition is detected, the µModule regulator rapidly initiates several simultaneous courses of action. An external MOSFET (MSP in Figure 3) disconnects the input supply, removing the high voltage path from the regulator and the high value load. Another external MOSFET (MCB in Figure 3) implements a low impedance crowbar function, quickly discharging the load's bypass capacitors (C_{OUT} in Figure 3). The LTM4641's built-in DC/DC step-down regulator enters a latched-off shutdown state and issues a fault signal indicated by the HYST pin which can be used by the system to initiate a well managed shutdown sequence and/or system reset. A dedicated voltage reference independent of the control loop's reference voltage is used to detect fault conditions. This provides resilience against a single-point failure, should the control loop's reference happen to fail.

The LTM4641's protection features are bolstered by its fault recovery options. In a traditional overvoltage fuse/SCR protection scheme, a fuse is relied upon to separate the power supply from the high value load. Recovery from a fuse-blowing fault requires human intervention—someone with physical access to the fuse to remove and replace it—introducing an unacceptable delay in fault recovery for high uptime or remote systems. In contrast, the LTM4641 can resume normal operation once the fault condition has cleared either by toggling a logic level control pin or by configuring the LTM4641 for autonomous restart after a specified timeout period. If fault conditions reappear after the LTM4641 resumes operation, the aforementioned protections immediately re-engage to protect the load.

INPUT SURGE PROTECTION

In some cases, output overvoltage protection alone is insufficient, and input overvoltage protection is required. The LTM4641's protection circuitry can monitor the input voltage and activate its protection features should a user-configured voltage threshold be exceeded. If the anticipated maximum input voltage exceeds the 38V rating of the module, input surge protection can be extended up to 80V with the LTM4641 still fully operational by adding an external high voltage LDO to keep control and protection circuitry alive (Figure 4).

CONCLUSION

Mission critical electronics increasingly mix a distributed power bus in the range of 12V–28V with low voltage high performance digital ICs. Risk mitigation has become more important than ever, particularly when the power bus is susceptible to voltage surges. The latest, costly FPGAs, ASICs, and microprocessors demand supply voltages with an absolute maximum limit as low as 3%–10% of the nominal voltage, making them extremely susceptible to damage, even fire from an overvoltage fault. Faults can be caused by timing errors in the switching regulator, an input voltage surge or improper components introduced during manufacture.

Overvoltage protection in mission critical systems must be fast, accurate and consistent—at levels beyond the capabilities of the traditional SCR/fuse-based scheme. The LTM4641 combines an efficient 10A DC/DC step-down regulator with a fast and accurate output overvoltage protection circuit in one surface mount package to meet demanding sytem requirements.

Visit www.linear.com/LTM4641 for data sheets, demo boards and other applications information. ■

Acknowledgements

- Afshin Odabaee, Product Marketing Manager, µModule Power Products, Linear Technology
- Yan Liang, Applications Engineer, Linear Technology

What's New with LTspice IV?

Gabino Alonso

video.linear.com/167

Follow @LTspice on Twitter for up-to-date information on models, demo circuits, events and user tips: *www.twitter.com/LTspice*

VIDEOS

Noise Simulations (video.linear.com/167)

Tyler Hutchison, Applications Engineer, shows how to setup an LTspice® .noise simulation to view both input and output referred voltage noise and discusses a couple of tricks to determining noise contributors.

SELECTED DEMO CIRCUITS

Boost & SEPIC Regulators

- **LT3957A:** High efficiency output boost converter (4.5V–16V to 24V at 600mA) www.linear.com/LT3957A
- **LTC3122:** 5V to 12V synchronous boost converter with output disconnect (1.8V–5.5V to 12V at 0.8A) www.linear.com/LTC3122
- **LTC3890-2:** Automotive 12V SEPIC and 3.3V step-down converter (5V–35V to 12V at 2A and 3.3V at 10A) www.linear.com/LTC3890-2

Buck-Boost Regulators

- **LT8705:** Telecom voltage stabilizer (36V–80V to 48V at 5A) www.linear.com/LT8705

Buck Regulators

- **LTC3838-2:** High efficiency step-down DC/DC converter with DCR current sensing (4.5V–14V to 0.4V–2.5V at 50A) www.linear.com/LTC3838-2
- **LTM8001:** Two output regulator with supercapacitor backup power (9V–15V to 3.3V at 1A & 2.5V at 0.5A) www.linear.com/LTM8001

Battery Chargers & LED Drivers

- **LT3651-8.4:** 4A, 2-cell charger with maximum power point control (16V–32V to 8.4V at 4A) www.linear.com/LT3651-8.2
- **LT3763:** 20A, pulse-width modulated, single LED driver (10V–30V to 6V LED at 20A) www.linear.com/LT3763

Cable Drop Compensators

- **LT6110:** Wire loss compensation using a current referenced LDO (4.9V–15V to 3V at 1A) www.linear.com/LT6110

PowerPath Controllers

- **LTC4417:** Priority switching from 12V main to 14.8V battery backup supply www.linear.com/LTC4417

SELECTED MODELS

Buck-Boost Regulators

- **LTC3129:** 15V, 200mA synchronous buck-boost DC/DC converter with 1.3µA quiescent current www.linear.com/LTC3129
- **LTC3245:** Wide V_{IN} range, low noise, 250mA buck-boost charge pump www.linear.com/LTC3245

Buck Regulators

- **LTC3621/-2:** 17V, 1A synchronous step-down regulator with 3.5µA quiescent current www.linear.com/LTC3621
- **LTC3639:** High efficiency, 150V 100mA synchronous step-down regulator www.linear.com/LTC3639
- **LTC3838-1/-2:** Dual, fast, accurate step-down DC/DC controller with dual differential output sensing www.linear.com/LTC3838-1
- **LTC3883/-1:** Single phase step-down DC/DC controller with digital power system management www.linear.com/LTC3883

Inverting & SEPIC Regulator

- **LTM8045:** Inverting or SEPIC µModule DC/DC converter with up to 700mA output current www.linear.com/LTM8045

What is LTspice IV?

LTspice® IV is a high performance SPICE simulator, schematic capture and waveform viewer designed to speed the process of power supply design. LTspice IV adds enhancements and models to SPICE, significantly reducing simulation time compared to typical SPICE simulators, allowing one to view waveforms for most switching regulators in minutes compared to hours for other SPICE simulators.

LTspice IV is available free from Linear Technology at www.linear.com/LTspice. Included in the download is a complete working version of LTspice IV, macro models for Linear Technology's power products, over 200 op amp models, as well as models for resistors, transistors and MOSFETs.

Battery Chargers

- **LT3651-8.2/8.4:** Monolithic 4A high voltage 2-cell Li-ion battery charger
  www.linear.com/product/LT3651-8.2

Cable Drop Compensators

- **LT6110:** Cable/wire drop compensator
  www.linear.com/LT6110

Hot Swap™ & PowerPath Controllers

- **LTC4226:** Wide operating range dual Hot Swap controller
  www.linear.com/LTC4226
- **LTC4417:** Prioritized PowerPath controller
  www.linear.com/LTC4417

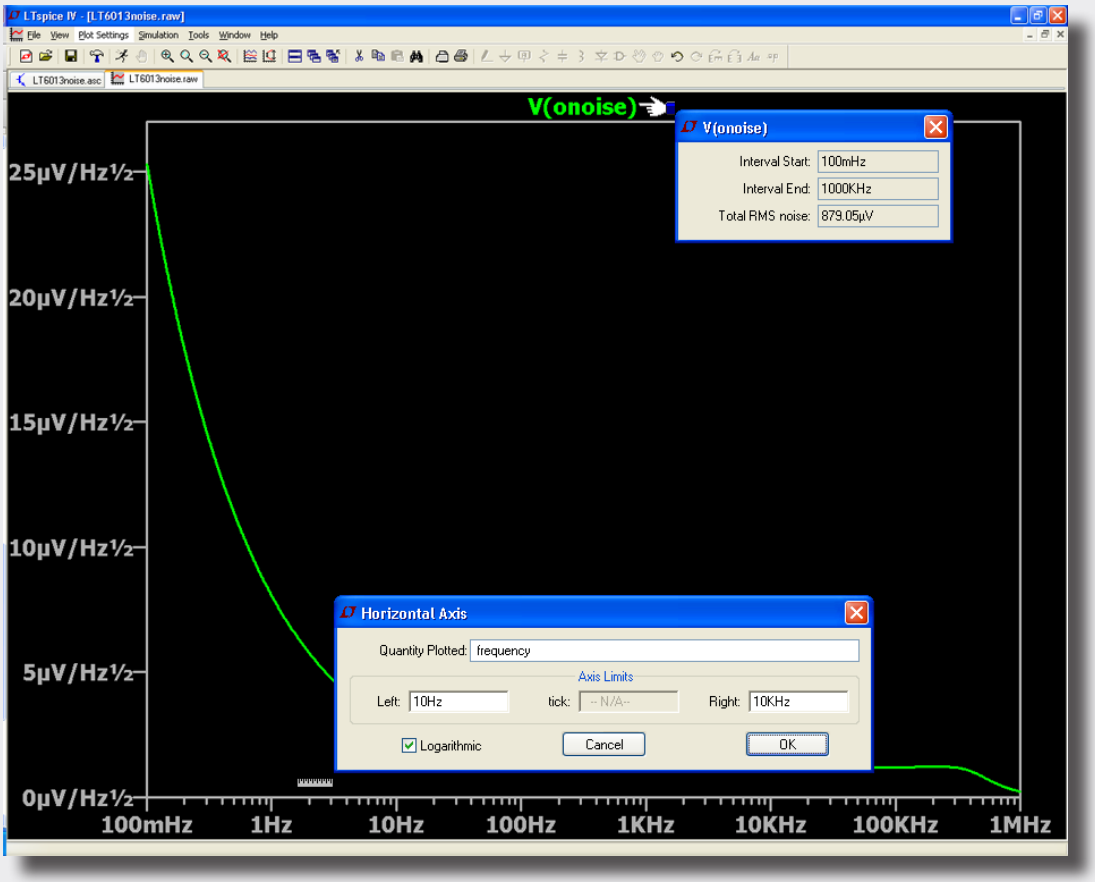
Oscillators

- **LTC6995-1/2:** TimerBlox®: long timer, low frequency oscillator
  www.linear.com/LTC6995 ■

Power User Tip

INTEGRATING NOISE OVER A BANDWIDTH

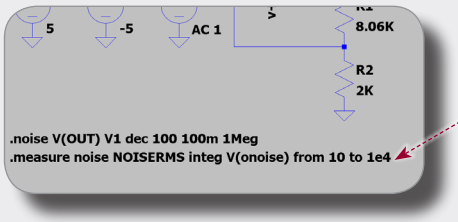
LTspice IV can perform .noise analysis of a circuit, where the noise voltage density (V/√Hz) for 1Hz bandwidth) can easily be plotted for the output noise, input noise or for any noisy component like a resistor, diode or transistor. (To learn more about how to perform a .noise simulation, check out Tyler Hutchison's noise simulation video at http://video.linear.com/167.)



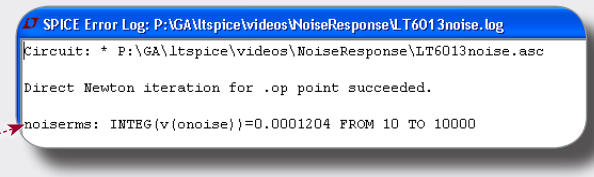
LTspice can also integrate noise over bandwidth. To use this feature, Ctrl-click the data trace label, V(noise), in the waveform viewer—the total RMS noise based on the bandwidth specified in the .noise directive is displayed.

If you prefer to calculate the total noise over a limited bandwidth rather than the bandwidth specified in the .noise directive you can modify the left (low) and right (high) frequency limits of the waveform viewer by clicking on the horizontal axis. Once you have your waveform displaying the bandwidth of interest, Ctrl-click the data trace label to display the total RMS noise based in the bandwidth of interest.

Alternately, you can add a .measure statement to your schematic that will calculate the total noise over a particular bandwidth, and view your results in the LTspice error log (Ctrl + L) after each simulation. (More information on using .measure statement can be found in LTspice Help (F1) and in the video at video.linear.com/115.)



Add a .measure statement to your scheme to produce calculated noise in the error log.



Happy simulations!

Reference Clock Distribution for a 325MHz IF Sampling System with over 30MHz Bandwidth, 64dB SNR and 80dB SFDR

Michel Azarian

Clock jitter introduced in an RF receiver through reference clock buffering and distribution can limit achievable system performance. The low jitter requirement is further exaggerated when a relatively high intermediate frequency (IF) is used in an effort to reap the benefits of relaxed front-end filter requirements. This article details the design of a 325MHz IF sampling system and introduces a clock buffer and distributor that converts a sine wave reference signal into a pair of differential LVPECL clocks appropriate to drive high speed ADCs, and does so while minimizing introduced jitter.

SYSTEM DESCRIPTION

In an IF sampling (or undersampling) system, where the ADC performs the last stage of downconversion in an RF receiver, the higher the IF is, the less steep the image rejection filter in the RF front-end can be. This helps in reducing the filter cost, size and insertion loss, which further lessens the need for amplification, leading to even lower cost and power consumption. Figure 1 shows a typical RF receiver chain employing IF sampling.

The downside of designing a receiver with a relatively high IF is that system specifications become more susceptible to the degraded ADC performance while sampling a higher-frequency analog input signal. ADC spurious free dynamic range (SFDR), for instance, worsens with higher input frequencies. More importantly, the ADC aperture jitter and its clock jitter, combined, begin to define the achieved signal-to-noise ratio (SNR) while sampling faster inputs.

The effect of clock jitter can be demonstrated by comparing the voltage error magnitudes due to clock jitter while sampling two slewing signals, one with a higher slope than the other, using the same ADC and clock. This clock has the same amount of time jitter (t_J in s-RMS) while sampling the two signals as illustrated in Figure 2. The amount of uncertainty introduced due to clock jitter is indeed higher with the faster moving signal, and, hence, clock jitter is a major, if not dominant, error source limiting the SNR when the analog input has higher frequency content.

Therefore, it is fundamental to keep the jitter of the ADC clock, denoted as the IF sampling clock in Figure 1, as low as possible.

To avoid AM-to-PM noise conversion at the ADC clock input, the clock should have a high slew rate, ideally be a square wave. The clock input of the ADC performs the role of a limiter, taking in a signal and squaring it by making decisions at the input signal's zero (or some other reference) crossings. AM-to-PM noise conversion occurs when the incoming signal has a slow slew rate, like in a low frequency and/or amplitude sine wave, where the signal goes through the zero crossings what resembles slow motion as compared to a square wave. If there is any type of AM noise, for example, resistor thermal noise, coupled noise from the power supplies, etc., the zero crossings of the incoming signal become inconsistent between consequent edges, leading to the creation of jitter at the limiter's output; thus, AM noise is converted into PM noise. Whereas, and if the incoming signal rushes through the zero crossing, as an LVPECL signal would normally do due to its fast rise and fall times, the AM noise added to the clock has no or very little chance of being converted into PM noise.

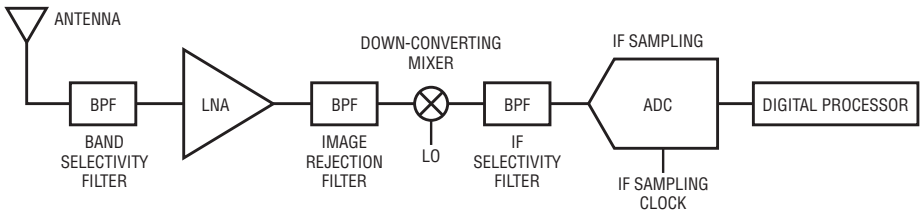
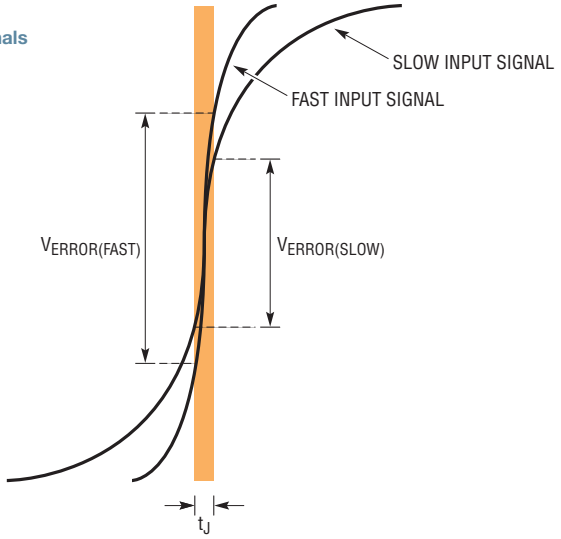


Figure 1. A typical single-IF-stage RF receiver block diagram

The downside of designing a receiver with a relatively high IF is that system specifications become more susceptible to the degraded ADC performance while sampling a higher-frequency analog input signal. ADC spurious free dynamic range (SFDR), for instance, worsens with higher input frequencies. More importantly, the ADC aperture jitter and its clock jitter, combined, begin to define the achieved signal-to-noise ratio (SNR) while sampling faster inputs.

Figure 2. Effect of clock jitter while digitizing slow and fast slewing signals



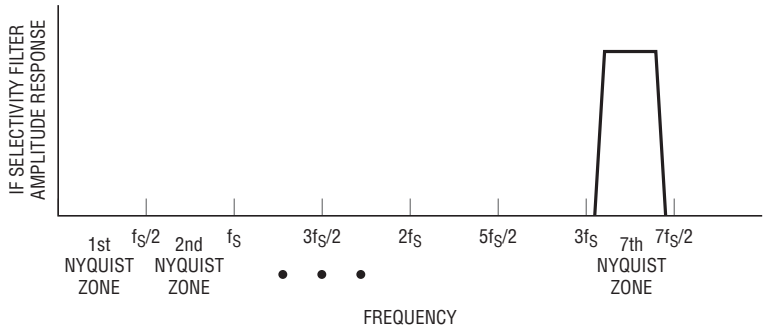
Also, most modern ADCs require their clock input to be driven differentially to attain their optimal performance. The clock signals are commonly routed on the PCB for quite some distance since their source and destination are usually not located close to each other. Running the clock signals in differential form makes them immune to coupling and leads to an overall more robust design as compared to single-ended clock routing.

The LO signal shown in Figure 1 is typically generated from a phase-locked loop (PLL) system. The PLL requires a reference clock to lock the LO to. Traditionally, 10MHz had been a common reference frequency. However, much higher frequency reference clocks are becoming more widespread nowadays. As a matter of fact, 100MHz and higher frequencies are not uncommon in modern RF designs.

The reference clock is usually generated from an OCXO or a TCXO device, which typically has very low jitter (or phase noise). If the PLL reference clock's frequency is chosen to be reasonably higher than twice the received RF channel's bandwidth (or that of multiple channels in a receiver where two or more adjacent channels are digitized simultaneously), the same reference signal can also be used to clock the IF sampling ADC, following some proper frequency planning. Ideally, the IF selectivity filter's passband and the majority of its transition zone should fit into a single Nyquist zone of the ADC to avoid frequency folding. This point is clarified with the help of the IF filter amplitude response given in Figure 3, where the IF is chosen to match the 7th Nyquist zone of the ADC. In Figure 3, f_S stands for the sampling rate of the ADC. In this case, the LO in Figure 1 would be chosen such that the down-converted signal output of the mixer is centered in the middle of the IF selectivity filter shown in Figure 3.

Figure 4 summarizes the clock distribution scheme discussed above assuming a reference frequency of 100MHz. The clock buffer and distributor of Figure 4 has a very important role in this system as it receives a single-ended sine wave from the OCXO or TCXO device, and delivers two differential LVPECL signals suitable for routing to the ADC and the PLL. It should do so

Figure 3. An example of an IF filter amplitude response with respect to ADC sampling rate that avoids frequency folding



The LTC2153-14 is a 310Msps, 14-bit ADC that is well-specified for high analog input frequencies, making it suitable as the IF sampling ADC in this application.

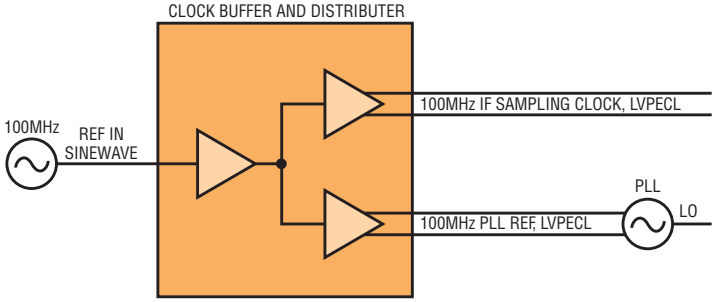


Figure 4. The reference clock distribution scheme

while adding a minimum amount of jitter to the distributed clock. The LTC6957-1 is a low additive jitter dual LVPECL output clock buffer that suits this application and meets all the requirements set forth in the discussion above. Other output formats can be achieved by employing different versions of the LTC6957. The LTC6957-2 has LVDS outputs and the LTC6957-3 and LTC6957-4 offer CMOS outputs.

CIRCUIT IMPLEMENTATION

As already discussed, jitter is one of the main limiting factors for increasing the IF. To find out what type of a performance can be achieved using a common ADC along with the LTC6957-1 as the clock distributor, two Linear Technology demonstration circuits are modified and hooked up as shown in Figure 5.

The LTC2153-14 is a 310Msps, 14-bit ADC that is well-specified for high analog input frequencies, making it suitable as the IF sampling ADC in this application. Its demonstration circuit, the DC1565A-G, is modified as shown in Figure 5.

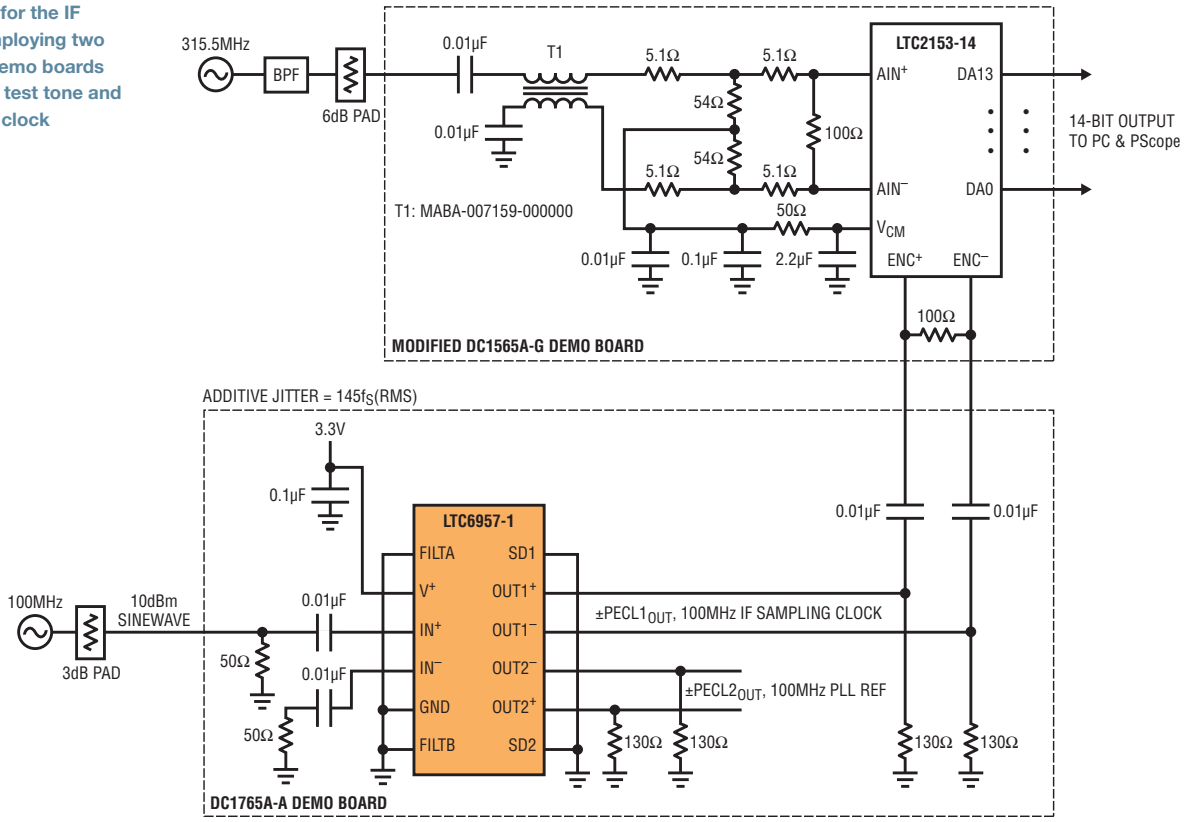


Figure 5. Schematic for the IF sampling system employing two Linear Technology demo boards with input 315.5MHz test tone and a 100MHz reference clock

The demonstration circuit, DC1765A-A, featuring the LTC6957-1, is used to buffer the sine wave output of a 100MHz OCXO. One of the DC1765A-A differential LVPECL output pairs is connected to the differential encode clock input of the DC1565A-G. The second pair could be used as the reference input of the LO generating PLL shown in Figure 1.

Given the ADC is clocked at 100MHz, the highest theoretical bandwidth that can be achieved, while avoiding aliasing, is 50MHz. As shown in Figure 3, the 7th Nyquist zone is picked, meaning that this 50MHz ideal bandwidth covers the 300MHz to 350MHz frequency range. This would require an ideal brick-wall bandpass filter centered at 325MHz with a passband of 50MHz to pass only the IF information present in the 300MHz to 350MHz range while rejecting everything else that could alias and interfere with the desired band.

Due to non infinitesimal transition zone between the filter passband and band-reject regions in a practical filter, besides center frequency tolerance, a more reasonable IF bandwidth selection in this case would be, for instance, a surface acoustic wave (SAW) filter with up to 30MHz bandwidth centered around 325MHz. SAW filters in this frequency range are becoming more readily available.

PERFORMANCE SUMMARY

A 315.5MHz test tone is connected to the analog input of the modified DC1565A-G through a BPF that resembles the IF selectivity filter and an attenuator to dial the amplitude seen by the ADC to –1dBFS.

Calculation of the LTC6957-1 Additive Jitter

In a sampling system, jitter is usually measured through a 2-step process. The first step is to take a baseline SNR measurement with a relatively low frequency analog input tone at –1dBFS where jitter is not a major contributor of noise. Call this measurement SNR_BASE. A second measurement is taken using the same sampling clock source as in the first reading but with a higher-frequency analog input tone, still at –1dBFS. The SNR should degrade with the second measurement if the input frequency is high enough to realize jitter-related SNR degradation. Call this second measurement SNR_DEGRADED. It should be noted that in the second measurement, jitter can have multiple sources, including the sampling clock, the ADC aperture jitter and the analog input signal. Taking the RMS difference of the two measurements results in the jitter-limited SNR achieved at the higher input frequency had the ADC had no quantization or thermal noise at its analog input. Call this calculated number SNR_JTTR. These three terms are related as such:

$$SNR\_JTTR = -10\log_{10}\left[10^{-\left(\frac{1}{10}SNR\_DEGRADED\right)} - 10^{-\left(\frac{1}{10}SNR\_BASE\right)}\right]$$

The achieved SNR (SNR_JTTR) due to t_J amount of total jitter at the encode input of the ADC for an analog input tone at a frequency f_{IN} is:

$$SNR\_JTTR = -20\log_{10}(2\pi f_{IN} t_J)$$

Combining the last two equations and solving for t_J results in an equation that calculates the system jitter directly from the two measurement outcomes mentioned above.

$$t_J = \frac{10^{\frac{1}{2}\log_{10}\left[10^{-\left(\frac{1}{10}SNR\_DEGRADED\right)} - 10^{-\left(\frac{1}{10}SNR\_BASE\right)}\right]}}{2\pi f_{IN}}$$

The LTC6957-1's jitter contribution is measured following the procedure outlined above. Two sets of measurements are taken based on the schematic shown in Figure 5. The first measures the total intrinsic system jitter, which includes the ADC's aperture jitter and these for the 100MHz and 315.5MHz sources but excluding the LTC6957-1. The second includes the LTC6957-1's noise contribution. Taking the RMS difference between the two measurements results in the LTC6957-1's additive jitter.

The total intrinsic system jitter excluding the contribution from the LTC6957-1 is found by connecting the 100MHz, 13dBm source straight into the encode input of the ADC with the use of a transformer to drive the clock input differentially. Two SNR measurements, excluding harmonics, are taken: one with a 10MHz, –1 dBFS sine wave at the analog input of the ADC, which reads 67.8dB. The second SNR measurement is taken with a 315.5MHz, –1 dBFS tone at the analog input of the ADC, resulting in 65.3 dB of SNR. The formula derived above calculates the total intrinsic system jitter:

$$\text{TOTAL INTRINSIC SYSTEM JITTER} = \frac{10^{\frac{1}{2}\log_{10}\left[10^{-\left(\frac{65.3}{10}\right)} - 10^{-\left(\frac{67.8}{10}\right)}\right]}}{2\pi \bullet 315.5M} = 181 f_S\,(\text{RMS})$$

The total system jitter after adding the LTC6957-1 to the system as shown in Figure 5 is found by taking another similar set of two measurements, one with an analog input of 10MHz and another with an analog input of 315.5MHz as described in the previous paragraph. The two SNR numbers are 67.8 dB and 64.24 dB, respectively. Using the same jitter formula as above results in the total system jitter:

$$\text{TOTAL SYSTEM JITTER} = \frac{10^{\frac{1}{2}\log_{10}\left[10^{-\left(\frac{64.24}{10}\right)} - 10^{-\left(\frac{67.8}{10}\right)}\right]}}{2\pi \bullet 315.5M} = 232 f_S\,(\text{RMS})$$

Taking the RMS difference between the intrinsic and total system jitter numbers gives the additive jitter contribution of the LTC6957-1:

$$\text{LTC6957-1 ADDITIVE JITTER} = \sqrt{232^2 - 181^2} = 145 f_S\,(\text{RMS})$$

The low jitter clock buffer and distributor, LTC6957-1, is employed to distribute the 100MHz system reference clock in LVPECL format to be used as the ADC sampling clock and the PLL reference. Performance of the IF sampling system is measured by looking at the SNR and SFDR numbers. An excellent 64dB of SNR and outstanding 80dB of SFDR are achieved with this system, enabling the relatively high IF sampling which helps relax the RF image rejection filter requirements.

The DC1565A-G is connected via USB to a PC, where PScope[1] data acquisition control software is used to look at two crucial parameters that affect the quality of the receiver: SNR and the SFDR. Figure 6 shows PScope™ in action, displaying a 131072-point FFT along with some analysis while having the 315.5MHz, –1dBFS tone as the analog input of the ADC and the 100MHz LVPECL signal buffered by the LTC6957-1 as the ADC encode clock. As can be seen in Figure 6, the achieved SNR is over 64dB and the SFDR is over 80dB. These are excellent numbers for a 325MHz IF sampler.

Because the input of the LTC6957-1 is a 100MHz sine wave at +10dBm power into 50Ω, its internal bandwidth limiting filters (FILTA and FILTB), which help reduce the amount of added jitter when the input is low in amplitude and/or frequency, are both turned off per LTC6957 data sheet recommendation.

CONCLUSION

A 325MHz IF sampling system, as part of an RF receiver, is built and evaluated. The low jitter clock buffer and distributor, LTC6957-1, is employed to distribute the 100MHz system reference clock in LVPECL format to be used as the ADC sampling clock and the PLL reference. Performance of the IF sampling system is measured by looking at the SNR and SFDR numbers. An excellent 64dB of SNR and outstanding 80dB of SFDR are achieved with this system, enabling the relatively high IF sampling which helps relax the RF image rejection filter requirements. ■

Notes

1 PScope collects and analyzes data from the ADC in both time and frequency domains, and displays relevant parameters (available for download at www.linear.com).

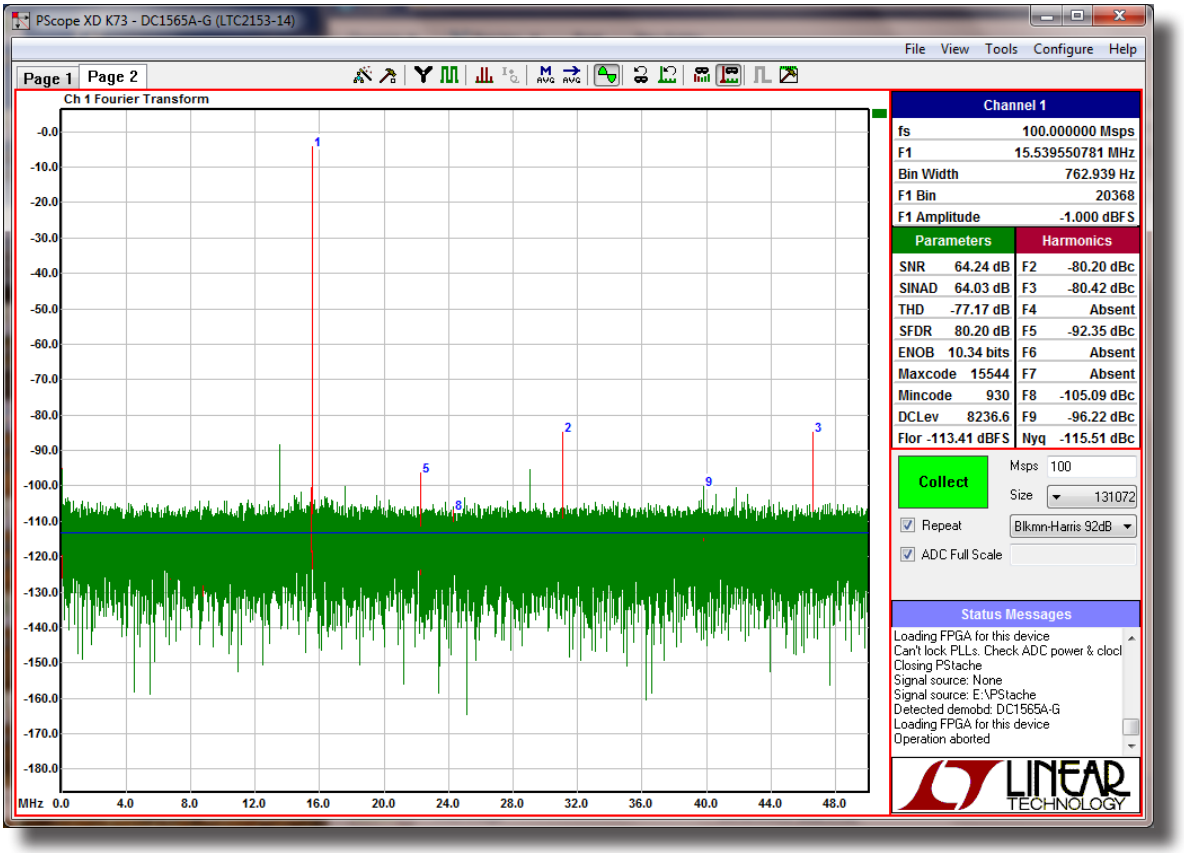


Figure 6. Screenshot of PScope showing the FFT and achieved signal integrity parameters of the system shown in Figure 5

Near Noiseless ADC Drivers for Imaging

Derek Redmayne

CCDs (charge coupled devices) and other sensors place heavy demands on digitizers, both in terms of sample rates, and in signal-to-noise ratio. The sensor output is typically a ground-referenced series of analog levels (pixels), possibly with transients occurring between the pixel boundaries. As the number of pixels increases, so does the sample rate of the ADC required to capture the image, with 20Msps pipelined ADCs sufficient for most high dynamic range applications. To ensure the highest SNR performance of the sampled signal, the drive circuitry for the ADC must provide low impedance, fast settling without introducing wideband noise and yet present high input impedance to the sensor.

This article presents an interface circuit between the sensor and a high performance ADC that does not compromise the SNR performance. The LTC2270 16-bit pipelined ADC family is intended for high end imaging applications. The 84.1dB SNR of this family makes it attractive for imaging, but it also features very good SFDR—over 100dB. The input range is $2.1V_{P-P}$, significantly less than the output of most imaging devices, so attenuation and level-shifting is required.

The inputs of these ADCs must be driven with a well-balanced differential drive. The single ended drive normally available from the sensor would force the internal virtual grounds to absorb common mode input current, which would cause degraded performance. These ADCs are also very low powered devices at 80mW/channel. Differential drive is actually fundamental to the low power operation since single ended drive would require additional power to maintain a stable internal reference point in the ADC. These devices operate on 1.8V supplies, imposing an input range of this order, if nothing else, simply to stay away from the rails. It is important to stay away from the rails to prevent differential phase error that would be associated with the voltage variable capacitance of internal protection diodes.

Therein lies a dilemma: A differential amplifier capable of performing single ended to differential translation without compromising the SNR of the ADC will necessarily have low input impedance (or low value resistors) and as it must settle quickly to 16-bit accuracy, will likely consume something on the order of four times the power of the ADC itself. The LTC6409 differential amplifier is an example that produces good results, but consumes 260mW, requiring that the surrounding network dissipate about 40mW just to produce a level shift. Furthermore, it dissipates signal power in the relatively low value resistors required for low noise and for maintaining phase margin.

These differential amplifiers as a result have low input impedance. The buffer that would be required to present a high impedance to the CCD also presents a dilemma. It must be low noise, be capable of settling in less than 25nsec, and be capable of slewing with enough dV/dt to maintain closed loop operation during transients. Additionally, it must be capable of driving the low input impedance of the differential amplifier. Yet, the application demands low power. This dilemma is even greater if there is the expectation that the amplifier operate from the single supply rail.

Most differential amplifiers present a number of problems as they either need band-limiting after the amplifier to the extent that settling is compromised, or they are not very stable with a gain of less than one (a noise gain of less than two) and as such tend to ring. Many are not common mode compatible with the 1.8V ADCs or they do not have enough headroom to accommodate a double terminated filter, or a level shift after the amplifier. The LTC6404 is a good case to study. It is stable at unity gain, does not ring as do some, and could potentially be used with an attenuator after the amplifier, but the input referred noise is 1.5nV. This compares to 1.1nV for the LTC6409. The LTC6404 noise density peaks considerably above 100MHz, it consumes 175mW, and it is not really compatible with the 900mV common mode required by the LTC2270. If it were followed by a filter

The LTC2270 16-bit pipelined ADC family is intended for high end imaging applications. The 84.1dB SNR of this family makes it attractive for imaging, but it also features very good SFDR—over 100dB. The input range is 2.1V_{P-P}, significantly less than the output of most imaging devices, so attenuation and level-shifting is required.

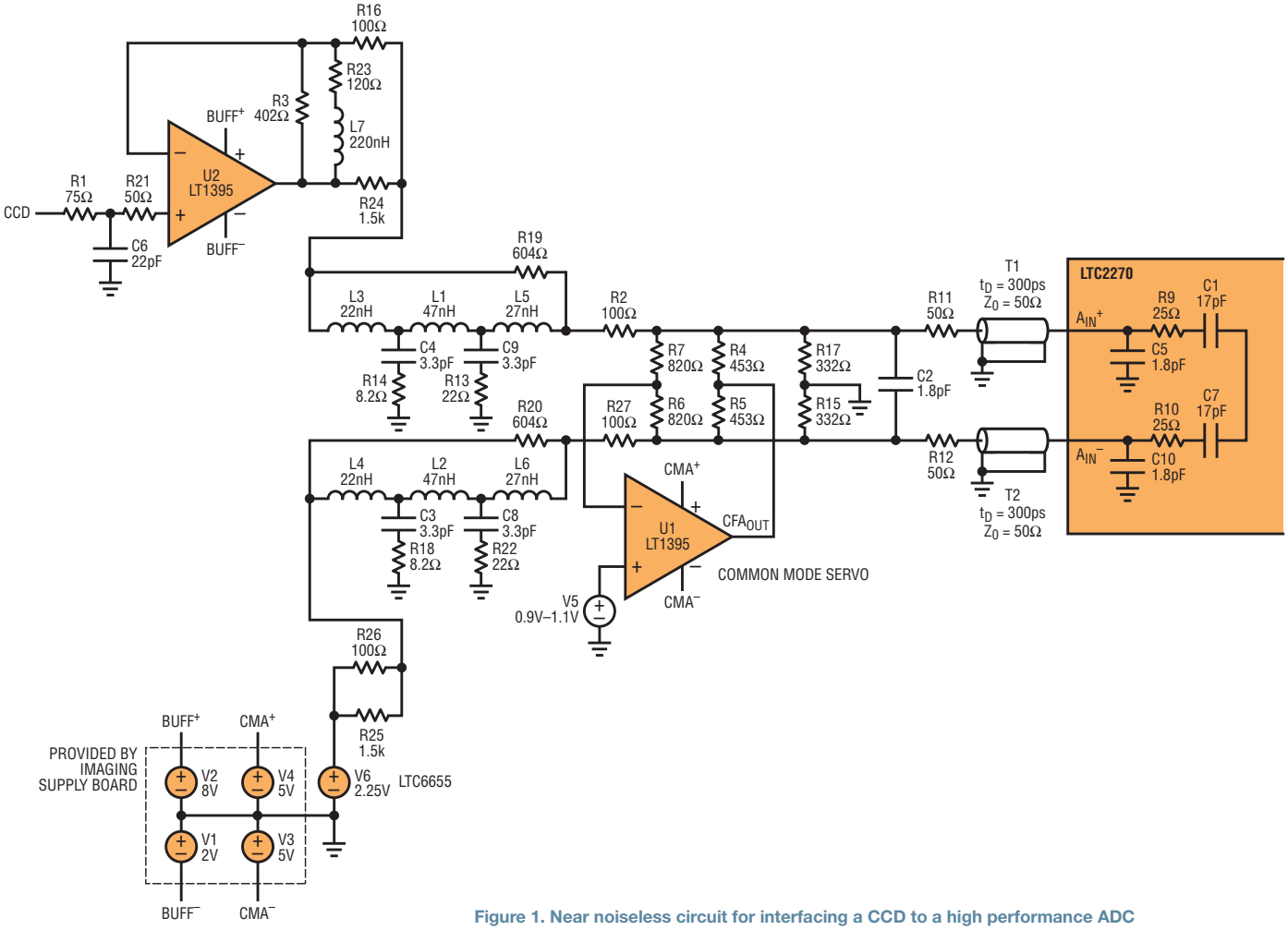


Figure 1. Near noiseless circuit for interfacing a CCD to a high performance ADC

and level shift, the impedance would be such that you will dissipate some 80mW dropping voltage in the dividers. You could potentially operate the amplifier off +3.3V and –2V to resolve common mode compatibility and produce a larger signal swing without requiring a level shift after the amplifier. But the negative supply is not often palatable to designers.

The settling time available to the amplifier may not be an entire clock cycle. The source may dictate this, but there is a disturbance produced by the ADC on the opposite edge of the clock and this would give the filter only ½-clock cycle to settle even if the amplifier were not otherwise disturbed. If the amplifier is disturbed by this event, it does not leave as much time for the filter to settle.

A simple RC would require about 14 time constants to settle to 16 bits, and for 20Msps, this would result in a bandwidth of about 90MHz. As it happens, the amplifier will be disturbed to some extent by sampling and this means that the bandwidth of a simple post filter must be extended to 130MHz to 150MHz to allow for some settling of the amplifier in response to the disturbance. Unfortunately, this will pass noise in the region where the amplifier is peaking. A higher order filter may result in a more pronounced reduction of noise contribution from

If an ADC with high SNR is required in an imaging application, a single-ended to differential conversion is required to get the signal from the CCD to the ADC. The conversion must attenuate the signal swing and provide a very stable common mode output level without adding significant noise.

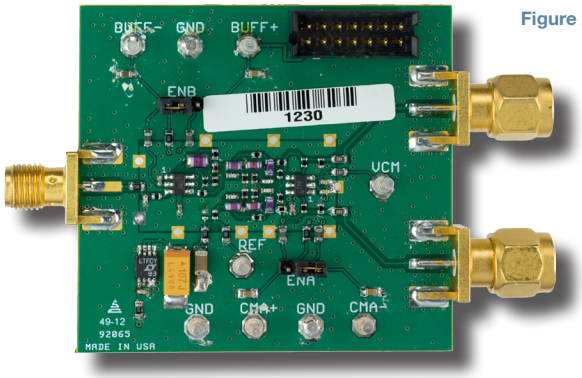


Figure 2. Prototype imaging board

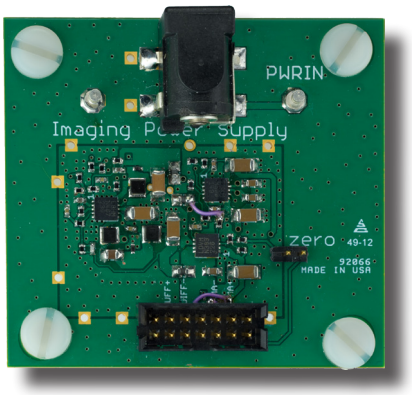


Figure 3. Prototype 0.5 square inch 4-output power supply

the earlier Nyquist zones, but will not necessarily settle very quickly.

The scheme described herein can drive the 25Msps LTC2270 family with 84.1dB SNR and 17pF sample capacitors. Impedances can be raised and power consumption can be reduced at sample rates of 20Msps, and less. For sample rates higher than 30Msps, a more conventional topology involving a fast buffer, followed by a differential amplifier like the LTC6409 is required. The LTC6404-1 can alternatively be used in that case.

THE NEAR NOISELESS SUGGESTION

The circuit in Figure 1 shows a suggested drive scheme that results in almost no loss of SNR with the LTC2270 family, yet can settle to 16 bits within 1 pixel at 25Msps. The noise at –84.0dB (all included) is such that it will not necessarily be within 1 count in a single frame, but averaging multiple frames could resolve to 16 bits.

The buffer amplifier (U2) is a current feedback amplifier used essentially as an emitter follower. The bulk of the output current is taken via R16, seemingly from the emitters, although power is delivered from the output.

As the impedance looking into the inverting input is low compared to the feedback network, the output noise is attenuated at the inverting input and, as a result, the inverting input noise current does not contribute significantly. This amplifier has a voltage noise specification of $4.5nV/\sqrt{Hz}$, although when used as a unity gain buffer, inverting input noise current in the minimum value feedback resistor produces $10.1nV/\sqrt{Hz}$. However in this emitter-follower-like mode of operation, it appears to be on the order of $1.5nV/\sqrt{Hz}$ to $2nV/\sqrt{Hz}$.

There is a feedback loop around the amplifier and this amplifier imposes a minimum feedback resistor of 400Ω. However, at low frequency, the feedback impedance is 400Ω in parallel with R23 to reduce the excursion required at the output. But at high frequency, the feedback is the required minimum 400Ω.

There is a minor amount of output power taken from the output, via R24, just to reduce the required excursion produced at the output. But this may not be required in many cases, for example where the video signal is 0V–4V, or less.

There is provision for R24 just in case, in the future, U2 may be a different amplifier where it is practical to take power from the output. There are several possible alternatives depending on required slewing. A low noise fast settling FET amplifier could possibly be used on a single supply. With rail-to-rail amplifiers, it is likely that the positive rail must be 6V to avoid crossing through the transition region between two input stages, a region that causes distortion. If the LT1395 is used, 7.5V to 8V must be used for V_{CC} and –2V for V_{SS}, if intended to receive 0V–5V signals.

A lower powered amplifier such as the LT6252 may be used if there is no need to settle through a full-scale step between pixels. Bad pixels however would bleed into following pixels. The presence of clock feed-through and the actual settling time available may limit these choices.

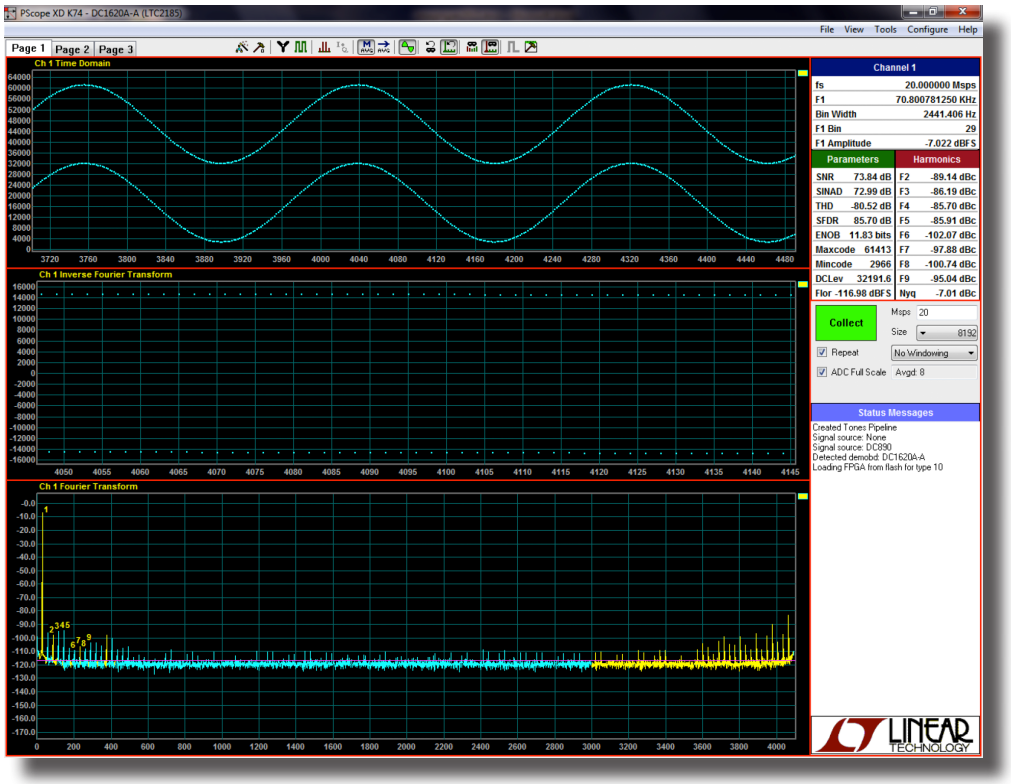


Figure 4. Two tone test –7.022dBfs sinusoid at 70kHz, –7.01dB synchronous square wave at Nyquist

The second amplifier is also an LT1395, but note that this cannot be a dual LTC1396, unless the application were to involve signals centered on ground potential. This second stage must operate on 5V and –5V in order to sink current and perform a level shift from ~2.5V common mode to 0.9V common mode, as well as provide differential drive by virtue of controlling the common mode. The noise and distortion contribution of this amplifier is largely rejected by the CMRR of the ADC as its influence is only common mode, assuming the network surrounding the amplifier is completely symmetrical.

We developed a power supply board that provides all four of the required voltages from a single 5V input. The power supply circuit is capable of powering four channels, yet produces no evidence of the 1.2MHz switching rate used by the LT3471—even at –125dBFS.

As shown, this driver produces 84.0dB SNR combined with the ADC and including any contribution from the power supply board. The tests below were done with R1 at 75Ω, and a 50Ω source. This circuit should be suitable where CCDs either have an output impedance in the 50Ω–200Ω range, or where the charge transfer into a holding cap produces an effective impedance in the hundreds of ohms. The use of a fast FET buffer may allow very high source impedance.

The capacitor C6, at 22pF, is required if the dV/dt during transients from the CCD exceeds the slew rate of the LTC1395 or if RFI is present. CCDs appear to tolerate capacitive loads of this magnitude. If the output stage of the LTC1395 is not capable of keeping up, conduction of input protection diodes would greatly reduce the input impedance. This conduction occurs in almost any feedback amplifier. And this would produce an error if a charge transfer mechanism were exposed to this input current, possibly even if buffered in the CCD. R21 is potentially desirable as source termination if the distance between C6 and the amplifier were extended.

This topology is only practical with ADCs that have approximately $2V_{P-P}$ input range and where the CCD signal is on the order of 0V–4V or 0V–5V. This takes advantage of the attenuation that is required to produce the balun action by controlling the common mode. This is analogous to the transmission line balun where high common mode impedance between input and output ports results in balanced drive if symmetrically terminated to AC ground.

The filter as shown produces a Gaussian-like response, and is 3dB down at about 40MHz. The filter is replicated twice independently, in order to provide a symmetrical network that maintains the error contribution of U1 as common mode.

R7, R4, and R17 and their counterparts satisfy the requirements for stability of U1, produce attenuation of the 0V–5V signal to ±1V, and produce a level shift. These

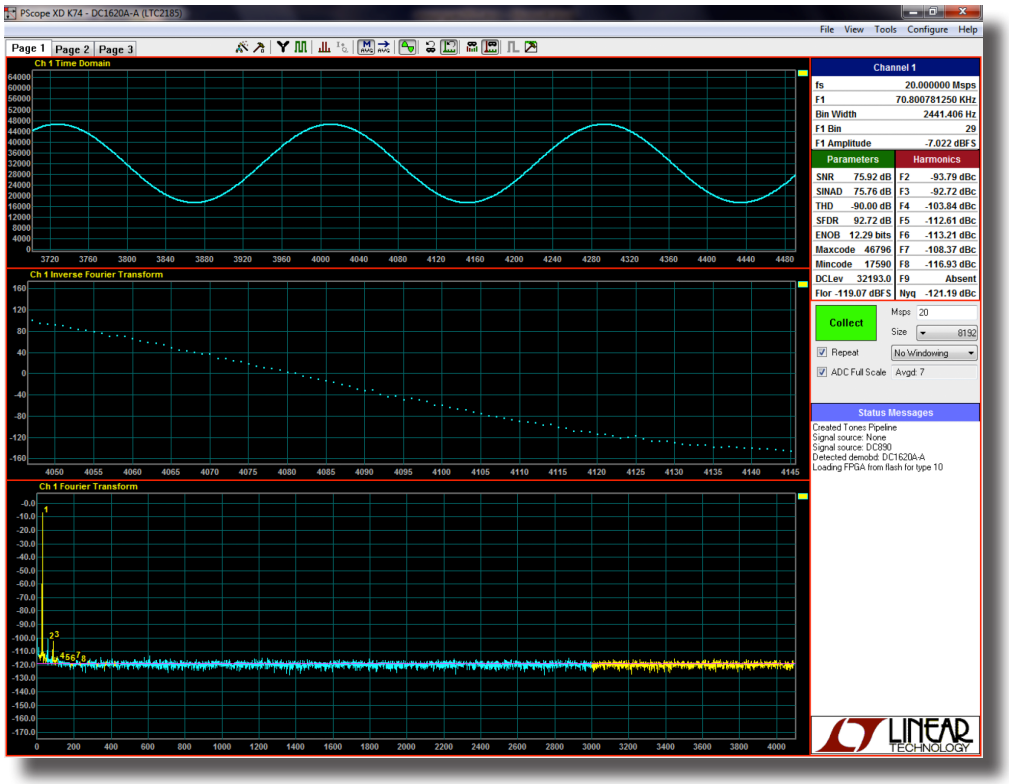


Figure 5. Same applied power level at 70kHz, but removal of power at Nyquist

elements can in fact be after the ADC and act as end termination, which allows somewhat faster settling. If there is a significant distance between the CCD and the ADC, simulation says that the transmission path can be extended between a pair of 50Ω resistors replacing R16. If the distance is between 30cm and up to about 60cm, the cable should be 75Ω. The source termination resistor would then be 75Ω and the other side, 25Ω. PCB traces should be higher than 75Ω if possible.

If this is intended to drive into the LTC2185, for example, a 350psec transmission path is possible. If the LTC2270 family is used, the 17pF sample capacitors require that this transmission line (T1 and T2 in Figure 1) should be less than 40psec (about 1cm).

Tests performed to satisfy that this will perform with CCD signals, besides digitizing small offset frequencies from ¼FS and ½FS at 20Msps and 25Msps, include: 300kHz –1dBFS sinusoid (–92dB SFDR 2nd and 3rd), representative of dV/dt in a CCD signal; as well as a near full scale square wave (10MHz and 5MHz) with a superimposed –20dB sinusoid at 200kHz, showing no distortion on the sinusoid resulting from the large synchronous excursion in pairs of "black and white pixels."

Note the appearance of two waveforms in the time domain plot in Figure 4, caused by alternation between the two levels in the square wave every other sample.

The inverse FFT window is zoomed in on the time axis, showing only the tone at Nyquist, this by selectively masking out the power in the 70kHz area.

Figure 5 shows no apparent power change in the low frequency tone, still at –7.022dBFS and only relatively minor change in the distortion components. This proves the addition of a high amplitude square wave is not causing compression at the peaks. A 70kHz tone, superimposed on a ½FS square wave is believed to represent the dV/dt and settling scenario that would be representative of that seen in a CCD waveform sampled near the end of the pixel.

CONCLUSION

If an ADC with high SNR is required in an imaging application, a single-ended to differential conversion is required to get the signal from the CCD to the ADC. The conversion must attenuate the signal swing and provide a very stable common mode output level without adding significant noise. The circuit presented here can do just that. Working with a low power ADC that has a data sheet SNR specification of 84.1dB, this circuit achieved 84.0dB—implying that the conversion was nearly noiseless. ■

Low Power, DC Accurate Drivers for 18-Bit ADCs

Guy Hoover

A common misconception about 18-bit SAR ADCs is the only way to drive them is with a high powered, high speed, low noise op amp or differential driver whose DC performance often leaves much to be desired. It is possible to use a low power, DC accurate op amp to drive an 18-bit SAR ADC if the input is a DC or low bandwidth AC signal and the op amp outputs are given sufficient time to settle. Using the single-ended to differential driver of Figure 1, four different low power dual op amps were tested to show the trade-offs in using low power drivers.

This circuit enables the testing of offset voltage, the maximum sample rate for DC and AC signals, noise and power consumption. The ADC used is the LTC2379-18, a 1.6Msps 18-bit SAR ADC with an offset of ±9LSBs, INL of ±2LSBs and peak-to-peak noise of 5LSBs.

The four amplifiers used are the LT1013, LTC6078, LTC6081 precision and LTC2051HV zero-drift dual op amps—Table 1 shows a summary of their major specs. The circuit supply voltage is the voltage applied to the V^+ and V^- terminals of the op amps. This voltage determines the power dissipation of the amplifier and its maximum signal swing. The voltages were chosen to maximize undistorted signal swing without exceeding the maximum ratings of the amplifiers or unnecessarily increasing power dissipation.

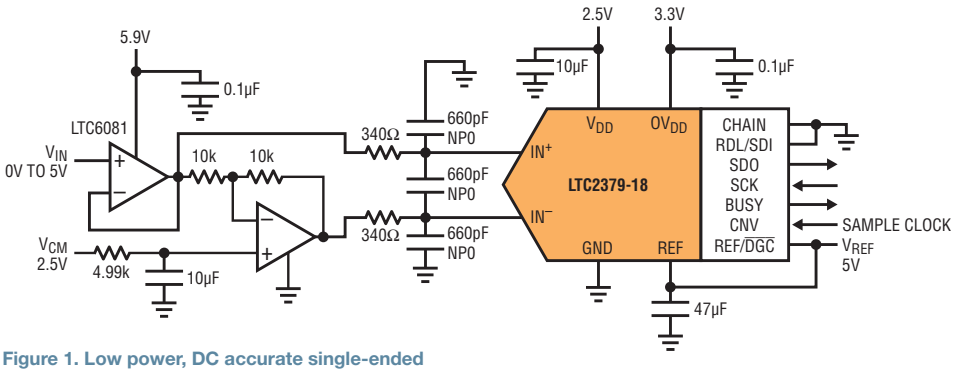


Figure 1. Low power, DC accurate single-ended to differential driver for the LTC2379-18

OFFSET VOLTAGE

The worst-case offset of the LTC2379-18 is only ±340µV. As Table 1 shows, the offset voltage of these four op amps is even lower, varying from ±3µV max for the LTC2051HV to ±150µV max for the LT1013. To maintain this low level of offset voltage careful circuit design and layout practices are required. Examples of this include using the 4.99kΩ resistor in the positive input of the inverting amplifier to balance the input bias current created voltage drops and using symmetrical layout around the positive and negative inputs of the ADC, minimizing the effects of the parasitic elements.

Table 1. Op amp comparison

PART	I_{SY} (µA) TYP/AMP	V_{OS} (µV) MAX	CIRCUIT SUPPLY VOLTAGE(V)
LT1013A	350	±150	8, –3
LTC2051HV	1000	±3	8, –3
LTC6078	55	±30	5.9, 0
LTC6081	340	±70	5.9, 0

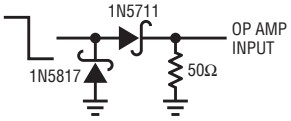
MAXIMUM SAMPLING RATE FOR DC SIGNALS

Even with a DC input voltage there is some settling time required. When the ADC goes from hold mode to sample mode, the sample capacitor is switched onto the analog input pin of the ADC producing a brief transient. The sample capacitor is then charged by the op amp back to its final value.

The maximum sampling frequency for a DC input voltage can be determined

The worst-case offset of the LTC2379-18 is only ±340µV. The offset voltage of the four op amps is even lower, varying from ±3µV max for the LTC2051HV to ±150µV max for the LT1013. To maintain this low level of offset voltage careful circuit design and layout practices are required.

Figure 2. Schottky diodes flatten falling edge of input pulse



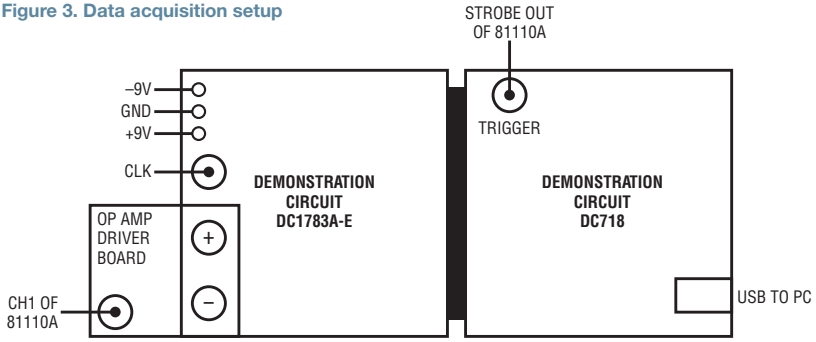
by reducing the sampling frequency until there is no ripple on the sampled waveform. Take this measurement with the analog input near positive or negative full scale as this typically causes the largest transients to be generated at the analog inputs, which in turn require the maximum settling time. Maximum sampling rates for the four op amps vary from 63ksps to 230ksps. The maximum sample rates for the four op amps are shown in Table 2.

MAXIMUM SAMPLING RATE FOR AC SIGNALS

For applications with a slow moving analog signal or a multiplexer at the driver input, determining the maximum sampling rate is more complex. With the potential for a full-scale swing from one measurement to the next it is necessary to consider the settling of the RC filter at the output of the driver circuit and the settling time of the op amp itself to an 18-bit level. Because settling to the 18-bit level is almost never specified, it must be experimentally determined.

Drive the op amps with a flat falling edge as shown in Figure 4 so that the settling of the op amps is measured; not the slow change of the DC input. The schematic for the edge shaping circuit is shown in Figure 2.

Figure 3. Data acquisition setup



It is important to keep the stray capacitance on the op amp input as small as possible to minimize the settling time of this circuit. By swapping the outputs of the SE-Diff driver circuit of Figure 1 it is possible to look at both falling and rising edge settling times.

With the flat input edge in place, one can look at the ADC output to see how long the output of the SE-Diff driver takes to settle. One method involves using the PScope data acquisition software and carefully choosing the sample rate and input frequency. Using a 50kHz sample rate to ensure that all four op amps settle completely once the input signal is constant would normally only allow a 20µs resolution in the settling time

Table 2. DC input maximum sampling rate

PART	DC INPUT MAXIMUM SAMPLE RATE (ksps)
LT1013A	185
LTC2051HV	230
LTC6078	63
LTC6081	165

measurement. By using the primitive wave capability of PScope and picking the sampling frequency, input frequency and sample size such that multiple passes of the input signal are sampled at different time slices it is possible to reassemble the samples to create a high resolution image of the input signal.

The formula used to determine the ratio of input frequency to sample frequency is

$$\frac{M}{N} \bullet f_S = f_{IN}$$

where N is the sample size. N must be 2^i where i is any integer from 10 to 17 for PScope. M is any odd number from 1 to N/2. f_S is the sample frequency and f_{IN} is the input frequency. Picking a sample size of 131072 to maximize resolution, an input frequency of 250Hz and M = 653 to get a sample rate of approximately 50ksps yields an f_S of 50.18070444ksps.

The full resolution shown is necessary, as the primitive wave requires an exactly coherent relationship between sample rate and input frequency. The clock and the input signal generator must be synchronized. Figure 3 shows the test

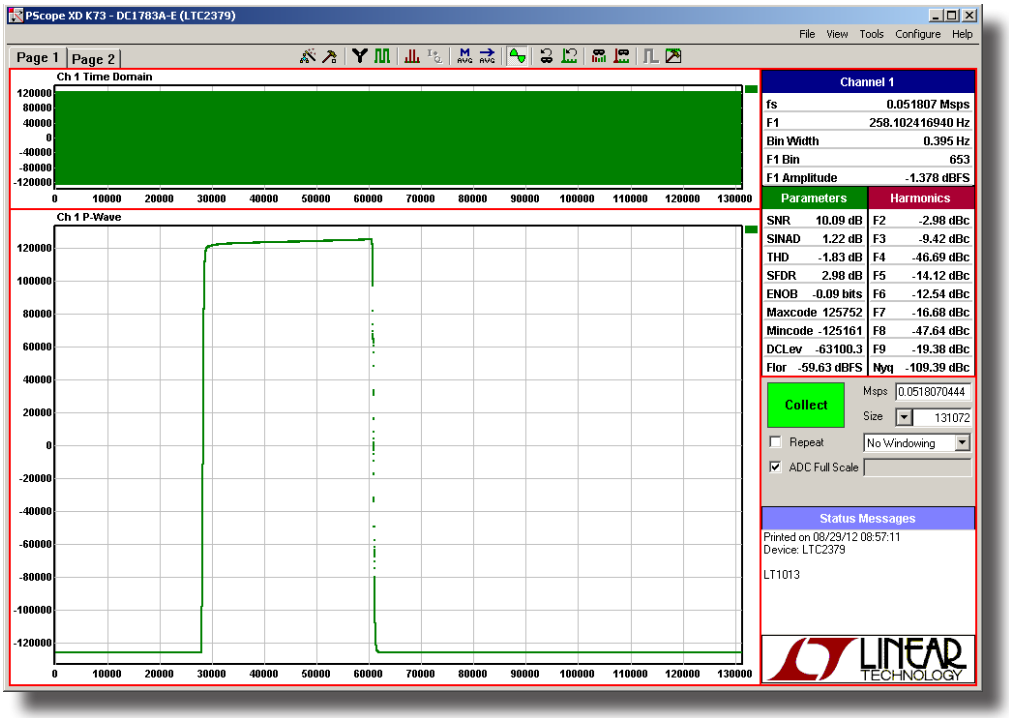


Figure 4. PScope primitive wave shows LT1013 settling time for falling edge with 30.5ns/sample resolution

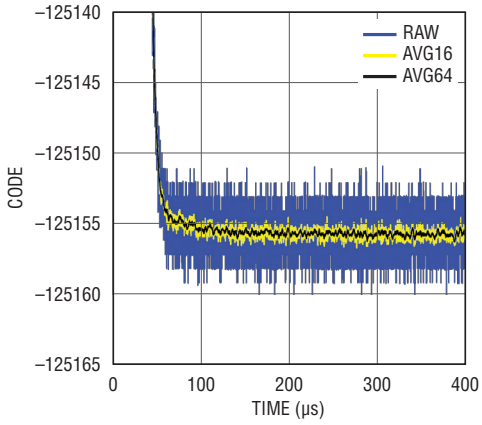


Figure 5. LT1013 settling

setup. The strobe signal makes sure that PScope starts capturing at the same point for each series of samples and requires that Start on Trigger is enabled in the Tools menu. To calculate the required clock frequency, multiply the desired sample frequency by 62 when using the DC1783A-E. This results in an input clock frequency of 3.111203675MHz.

The PScope output for the LT1013 is shown in Figure 4. With 131072 samples divided into the 4ms period of the input waveform, a resolution of 30.5ns/point is achieved. By zooming in on the start and stop points of the primitive waveform it is possible to calculate an approximate settling time. This is limited by the peak-to-peak noise. To increase the accuracy of this measurement, it is possible to take the raw data from PScope, export it to Excel or MATLAB, and then reassemble the primitive wave and average the resulting data. The raw results as well as the averages of 16 readings and 64 readings for the four op amps are shown in Figures 5–8. The settling times and peak-to-peak noise are summarized in Table 3. Note that the LTC2051HV, which had the fastest sample rate for a DC signal has the slowest settling time for a full scale input swing. This is a result of the time required to auto-zero the difference in offset voltage caused by the change in common mode input voltage.

Removing the Schottky diodes and driving a 20Hz sine wave into V_{IN} of the SE-Diff input with a sampling frequency of approximately 1/(settling time) yields the THD numbers for the circuit of Figure 1 shown in Table 4. Good THD numbers are an indication of the linearity of the circuit.

NOISE

As shown in the summary of Table 3, the combination of the SE-Diff driver and the LTC2379-18 yields a peak-to-peak noise that is 1.5 to 3 times higher than the ADC by itself. With relatively modest averaging it is possible to obtain noise levels that approach 1LSB peak-to-peak. As long as the noise is Gaussian and not caused by clock feedthrough or some other synchronous source, averaging should reduce the noise by the square root of the number of the samples. Averaging reduces the

Table 3. Settling times and peak-to-peak noise

PART	SETTLING TIME (µs)	PK-PK NOISE (LSBs)	AVERAGE OF 16 SAMPLES PK-PK NOISE (LSBs)	AVERAGE OF 64 SAMPLES PK-PK NOISE (LSBs)
LT1013	80	10	2.2	1.1
LTC2051HV	3000	14	2.9	1.2
LTC6078	140	12	3.3	1.7
LTC6081	130	8	1.8	0.9

Table 4. THD

PART	f_S (kHz)	THD (dB), A_{IN} = –1dBFS
LT1013	12.0	–105
LTC2051HV	0.3	–104
LTC6078	7.0	–98
LTC6081	7.0	–105

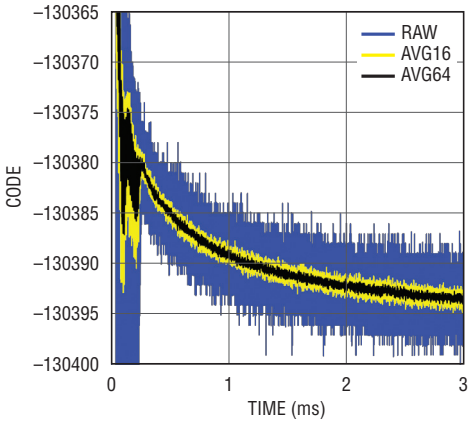


Figure 6. LTC2051HV settling

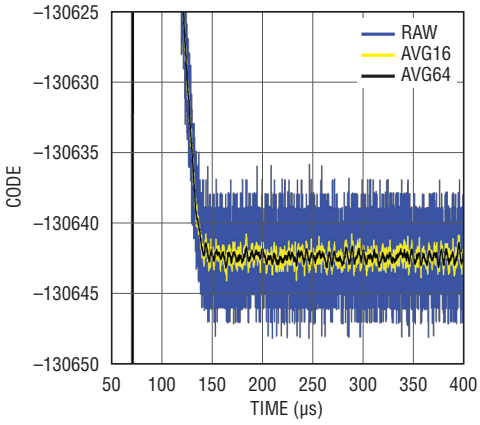


Figure 7. LTC6078 settling

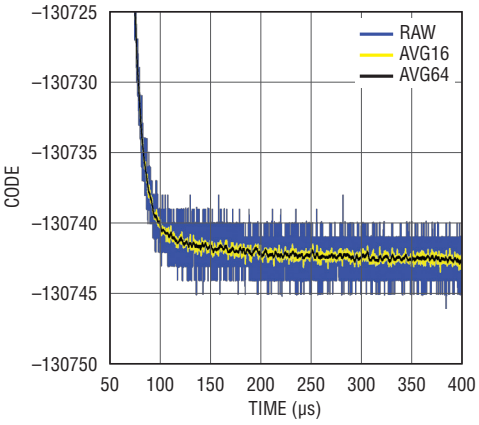


Figure 8. LTC6081 settling

effective sampling rate and may not be practical with non-repetitive AC signals.

POWER CONSUMPTION

Table 5 shows the power dissipation of the op amps and the LTC2379-18 at the maximum DC and AC sampling frequencies of the single-ended to differential data acquisition circuit of Figure 1. The op amp power dissipation is per amplifier and does not change with sampling frequency because the op amps are always on. The LTC2379-18 power dissipation is linear with sampling frequency due to its auto shutdown after a conversion. The combined circuit power dissipation in columns four and six of Table 5 shows the dissipation of the two op amps and the LTC2379-18 used in the circuit added together. At the higher sampling rates that are possible with DC input signals, the power dissipation of the LTC2379-18 is a significant portion of the total. At the lower sampling rates required for AC or muxed input signals, the op amps dissipate almost all of the power for this circuit.

CONCLUSION

Using low power, DC-accurate op amps to drive 18-bit SAR ADCs is possible as long as enough time is allowed for the op amps to settle. Settling time is the limiting factor in determining the circuit's maximum sampling rate, and varies greatly by op amp choice and the type of signal source, DC or AC. ADC offset and linearity can be maintained using low power op amps. Due to the higher noise of the low power op amps, some averaging may be required to reduce the noise at the expense of a lower effective sampling rate. At lower sample rates power dissipation is limited by the op amp driver circuitry, which must remain on so that it can settle, while the ADC can typically be powered down after only a brief conversion period. It is important to pick an op amp that is a good match to the offset, sampling rate, noise, linearity and power requirements of your overall circuit requirements. ■

Table 5. Power dissipation at maximum sampling frequencies for AC and DC input signals

PART	OP AMP P_D (mW) AT CIRCUIT SUPPLY VOLTAGE	LTC2379-18 P_D (mW) AT MAX DC f_S	COMBINED CIRCUIT P_D (mW) AT MAX DC f_S	LTC2379-18 P_D (mW) AT MAX AC f_S	COMBINED CIRCUIT P_D (mW) AT MAX AC f_S
LT1013	3.85	2.08	9.78	0.135	7.835
LTC2051HV	11.00	2.59	24.59	0.003	22.003
LTC6078	0.32	0.71	1.35	0.080	0.720
LTC6081	2.01	1.86	5.88	0.080	4.100

WIDE COMMON MODE RANGE 10X GAIN INSTRUMENTATION AMPLIFIER

The LTC6090 is a high voltage precision operational amplifier. The low noise, low bias current input stage is ideal for high gain configurations. The LTC6090 has low input offset voltage, a rail-to-rail output stage, and can be run from a single 140V or split ±70V supplies..

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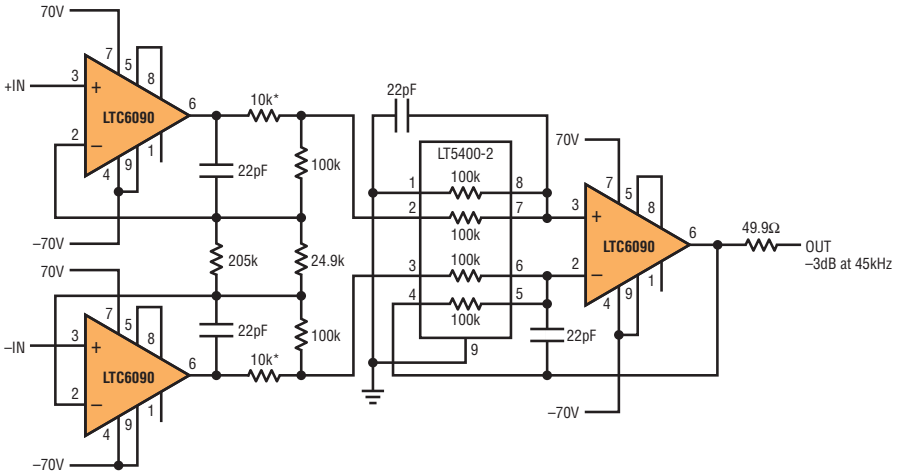

WIRE LOSS COMPENSATION USING A CURRENT REFERENCED LDO

This circuit shows a cable drop compensation circuit using a current referenced regulator, the LT3080. A precision 10µA set current, I_{SET}, is sourced through two series connected resistors to program the output voltage for the remote load. To compensate for the load connecting cable drop requires sourcing an additional current into this resistor pair to increase the output voltage. The LT6110 provides a sourced current at the IMON pin which is also directly proportional to the current flowing to the load. This current is three times the normal I_{OUT} current.

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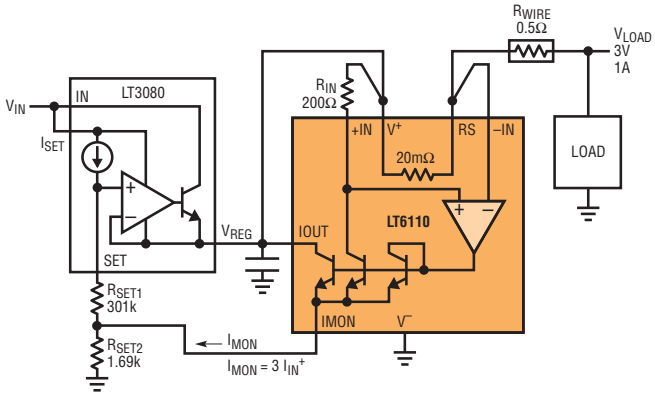

DUAL SUPERCAPACITOR BACKUP POWER SUPPLY, 0.5V TO 5V

The LTC3122 is a synchronous step-up DC/DC converter with true output disconnect and inrush current limiting. The 2.5A current limit along with the ability to program output voltages up to 15V makes the LTC3122 well suited for a variety of demanding applications. Once started, operation will continue with inputs down to 500mV, extending run time in many applications.

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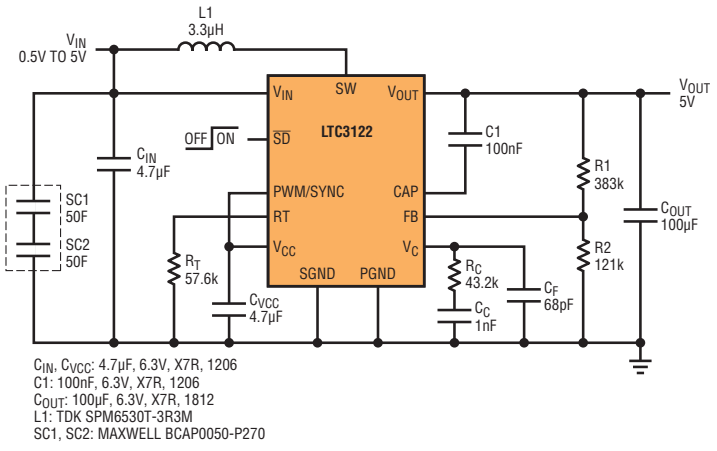

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